



- Tentative Specification
- Preliminary Specification
- Approval Specification

MODEL NO.: V645H1
SUFFIX: LE1

Customer:

APPROVED BY

SIGNATURE

Name / Title

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
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REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 0.0	Jan. 12,2012	All	All	The tentative specification was first issued.



1. GENERAL DESCRIPTION

1.1 OVERVIEW

V645H1-LE1 is a 64.5" TFT Liquid Crystal Display module with LED Backlight unit and 2ch LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display 1.07G colors (8-bit+hi-FRC). The converter module for backlight is built-in.

1.2 FEATURES

- High contrast ratio (5000:1)
- Fast response time (4ms)
- High color saturation (NTSC 70%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 240 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- Viewing Angle : 176(H)/176(V) (CR>20)
- RoHs compliance

1.3 APPLICATION

- Standard Living Room TVs
- Public Display Application
- Home Theater Application
- MFM Application

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1428.48 (H) x 803.52 (V) (64.5" diagonal)	mm	(1)
Bezel Opening Area	1440.6(H) x 814.6(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.248 (H) x 0.744 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.07G colors (8-bit+hi-FRC)	color	-
Display Operation Mode	Transmissive mode / Normally Black	-	-
Surface Treatment	Hard coating (Hardness:3H)	-	(2)

Note (1) Please refer to the attached drawings in chapter 11 for more information about the front and back outlines.

Note (2) The spec. of the surface treatment is temporarily for this phase. CMI reserves the rights to change this feature.

**1.5 MECHANICAL SPECIFICATIONS**

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	1472.3	1474.1	1475.9	mm	(1)
	Vertical (V)	849.1	850.6	852.1	mm	(1)
	Depth (D)	34	35	36	mm	(2)
	Depth (D)	28.8	29.8	30.8	mm	(3)
Weight		-	29600	-	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth is between bezel to T-CON cover.

Note (3) Module Depth is between bezel to converter cover.

2. ABSOLUTE MAXIMUM RATINGS**2.1 ABSOLUTE RATINGS OF ENVIRONMENT**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	°C	(1)
Operating Ambient Temperature	TOP	0	50	°C	(1), (2)
Shock (Non-Operating)	SNOP	-	35	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. ($T_a \leq 40\text{ }^{\circ}\text{C}$).

(b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40\text{ }^{\circ}\text{C}$).

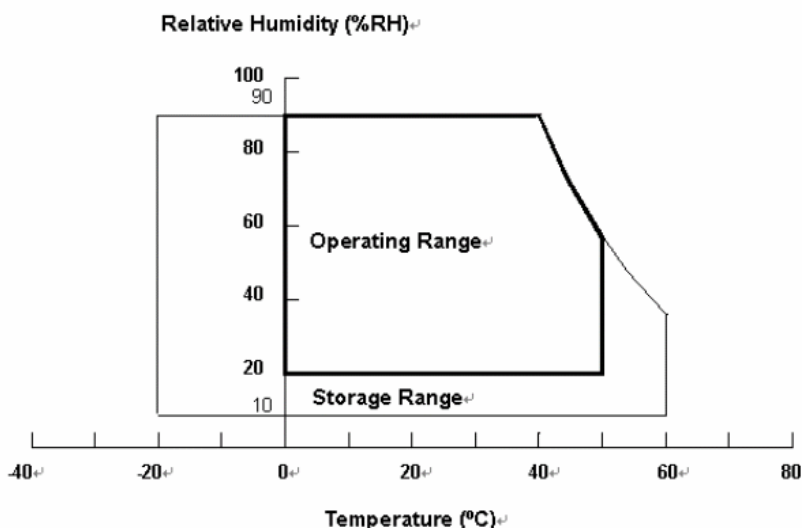
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for $\pm X$, $\pm Y$, $\pm Z$.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 °C at normal humidity without condensation.
- (b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS**2.3.1 TFT LCD MODULE**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

2.3.2 BACKLIGHT UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Light Bar Voltage	V _W	Ta = 25 °C	-	-	60	V _{RMS}	3D Mode
Converter Input Voltage	V _{BL}	-	0	-	30	V	
Control Signal Level	-	-	-0.3	-	7	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and External PWM Control

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

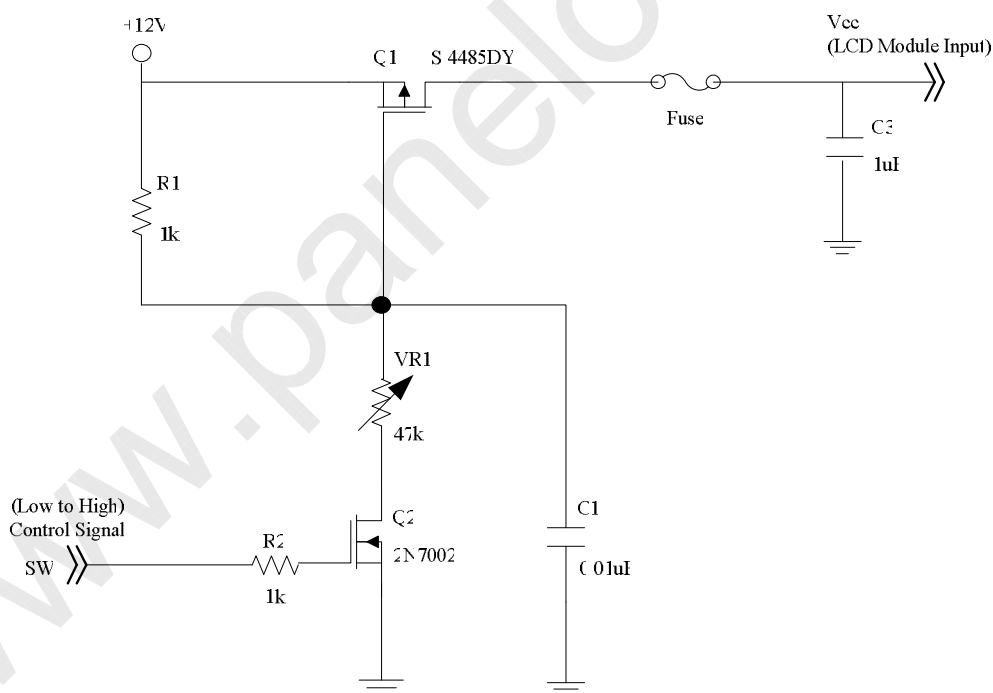
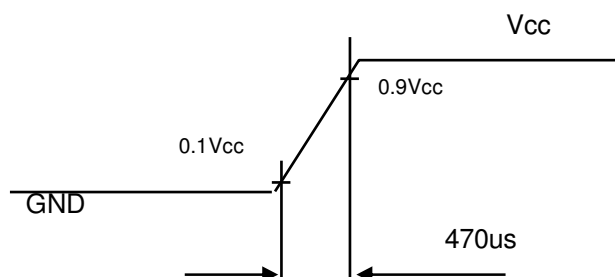
(Ta = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V _{CC}	10.8	12	13.2	V	(1)
Rush Current		I _{RUSH}	—	—	4.5	A	(2)
Power consumption	White Pattern	P _T	—	21	25.2	W	(3)
	Horizontal Stripe	P _T	—	41.64	51.24	W	
	Black Pattern	P _T	—	19.8	23.88	W	
Power Supply Current	White Pattern	—	—	1.75	2.1	A	(3)
	Horizontal Stripe	—	—	3.47	4.27	A	
	Black Pattern	—	—	1.65	1.99	A	
LVDS interface	Differential Input High Threshold Voltage	V _{LVTH}	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V _{LVTL}	—	—	-100	mV	
	Common Input Voltage	V _{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	V _{ID}	200	—	600	mV	
	Terminating Resistor	R _T	—	100	—	ohm	
CMOS interface	Input High Threshold Voltage	V _{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:

Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at $V_{CC} = 12\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 240\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



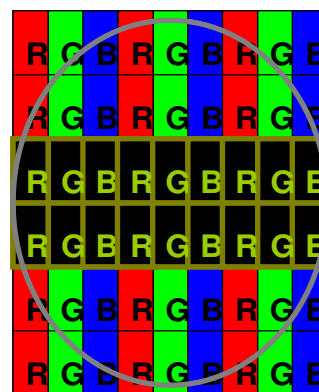
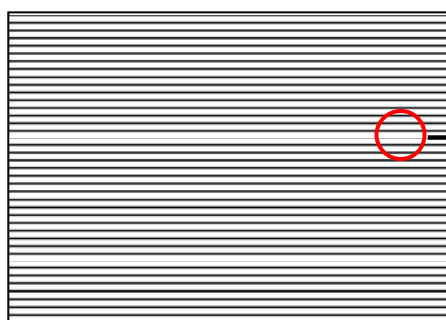
Active Area

b. Black Pattern

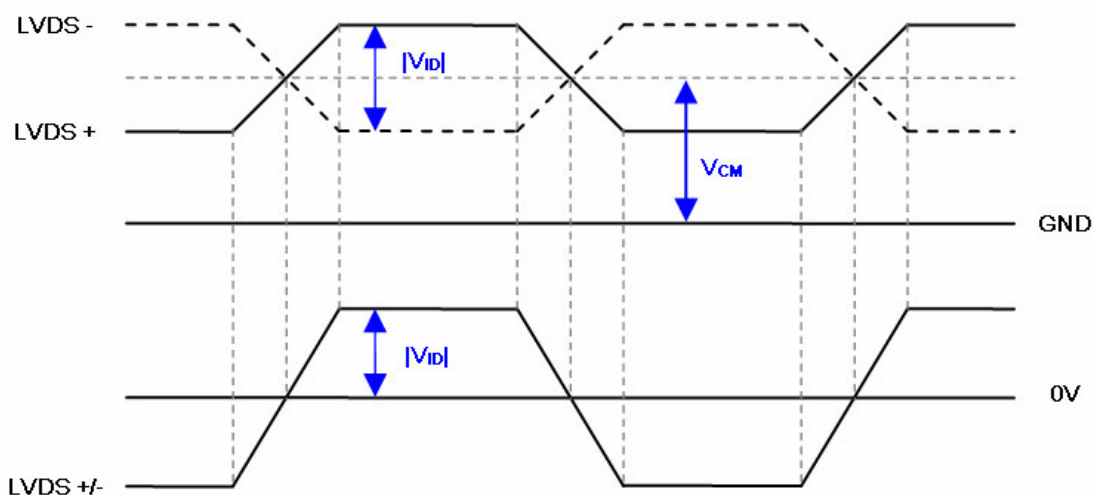


Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows:



3.2 BACKLIGHT CONNECTOR PIN CONFIGURATION

3.2.1 LED LIGHT BAR CHARACTERISTICS (Ta = 25 ± 2 °C)

The backlight unit contains 8pcs light bar.

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Total Current	If	4512	4800	5088	mA	32 String
One String Current	IL(2D)	141	150	159	mA	
	IL(3D)	-	450	-	mApeak	3D ENA=ON
LED Forward Voltage	Vf	2.8	3.2	3.6	V _{DC}	IL = 150mA
One String Voltage	VW	30.8	-	39.6	V _{DC}	IL = 150mA
One String Voltage Variation	ΔVW	-	-	2	V	For 1 BLU
Life time	-	30000	-	-	Hrs	(1)

Note (1) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value, Operating condition: Continuous operating at Ta = 25±2°C, IL = 150mA

3.2.2 CONVERTER CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P _{BL(2D)}	-	188	216.5	W	(1), (2) IL = 150 mA
	P _{BL(3D)}	-	140	164	W	(1), (2) IL=450mApeak.
Converter Input Voltage	VBL	22.8	24.0	25.2	V _{DC}	
Converter Input Current	IBL(2D)	-	7.83	9	A	Non Dimming
	IBL(3D)	-	TBD	TBD	A	
Input Inrush Current	IR(2D)	-	-	12.2	Apeak	V _{BL} =22.8V, (IL=typ.) (3), (6)
	IR(3D)	-	-	8.6	Apeak	V _{BL} =22.8V, (IL=3*typ.) (3), (6)
Dimming Frequency	FB	150	160	170	Hz	(5)
Minimum Duty Ratio	DMIN	5	10	-	%	(4), (5)

Note (1) The power supply capacity should be higher than the total converter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when converter dimming.

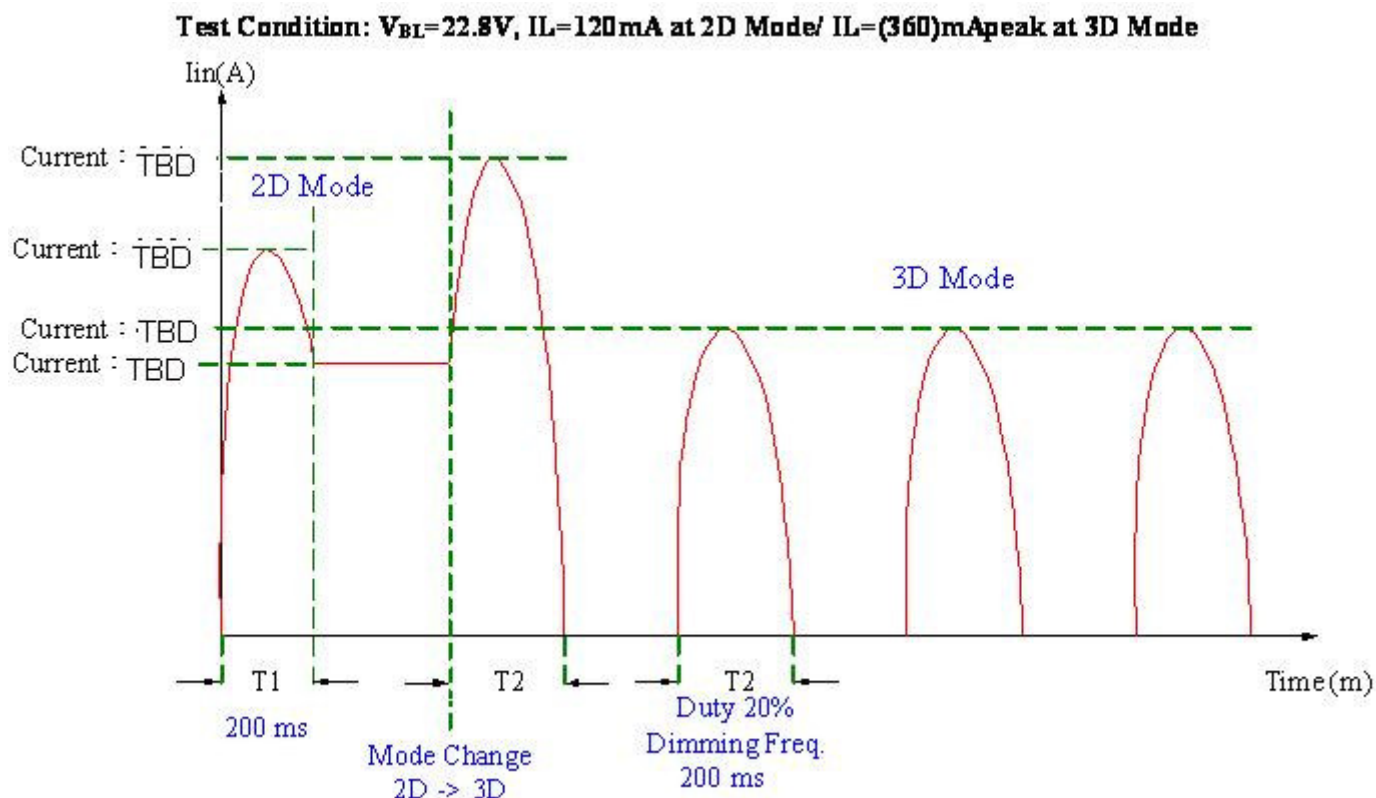
Note (2) The measurement condition of Max. value is based on 64.5" backlight unit under input voltage 24V, average LED current 150mA at 2D Mode (LED current 450mA_{peak} at 3D Mode) and lighting 1 hour later.

Note (3) For input inrush current measure, the VBL rising time from 10% to 90% is about 30ms.

Note (4) 5% minimum duty ratio is only valid for electrical operation.

Note (5) FB and DMIN are available only at 2D Mode.

Note (6) Below diagram is only for power supply design reference.



3.2.3 CONVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note	
				Min.	Typ.	Max.			
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V		
	OFF		—	0	—	0.8	V		
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.25	V	Duty on	(5), (6)
	LO		—	0	—	0.8	V	Duty off	
External PWM Frequency		F _{EPWM}	—	150	160	170	Hz	Normal mode	
Error Signal		ERR	—	—	—	—	—	Abnormal: Open collector Normal: GND (4)	
VBL Rising Time		Tr1	—	30	—	—	ms	10%-90%V _{BL}	
Control Signal Rising Time		Tr	—	—	—	100	ms		
Control Signal Falling Time		Tf	—	—	—	100	ms		
PWM Signal Rising Time		TPWMR	—	—	—	50	us	(6)	
PWM Signal Falling Time		TPWMF	—	—	—	50	us		
Input Impedance		Rin	—	1	—	—	MΩ	EPWM, BLON	
PWM Delay Time		TPWM	—	100	—	—	ms	(6)	
BLON Delay Time		T _{on}	—	300	—	—	ms		
		T _{on1}	—	300	—	—	ms		
BLON Off Time		Toff	—	300	—	—	ms		

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the Fig.1. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When converter protective function is triggered, ERR will output open collector status.

Note (5) The EPWM interface that inserts a pull up resistor to 5V in Max Duty (100%), please refers to Fig.2.

Note (6) EPWM is available only at 2D Mode.

Note(7): [Recommend] EPWM duty ratio is set at 100%(Max. Brightness) in 3D Mode.

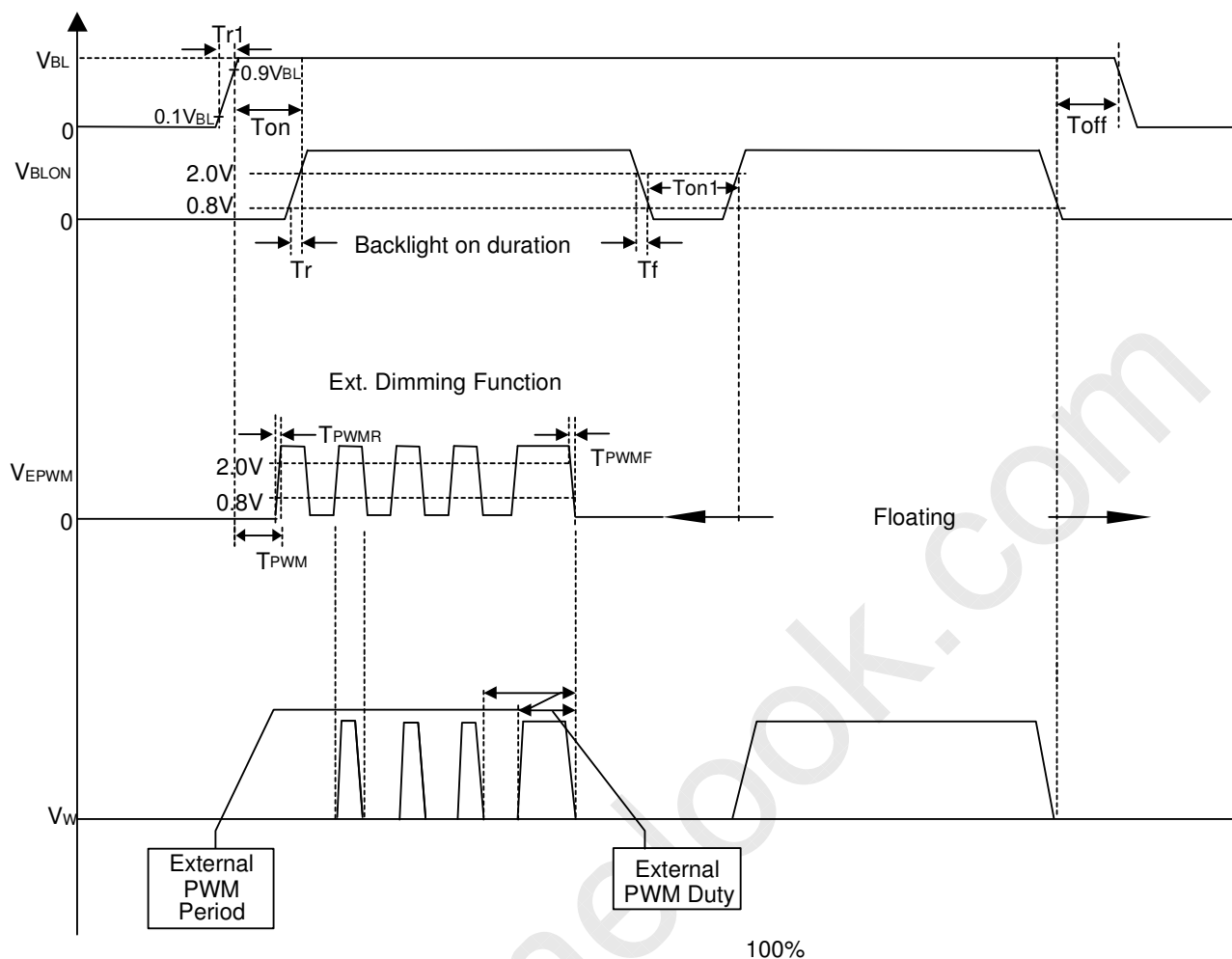


Fig. 1

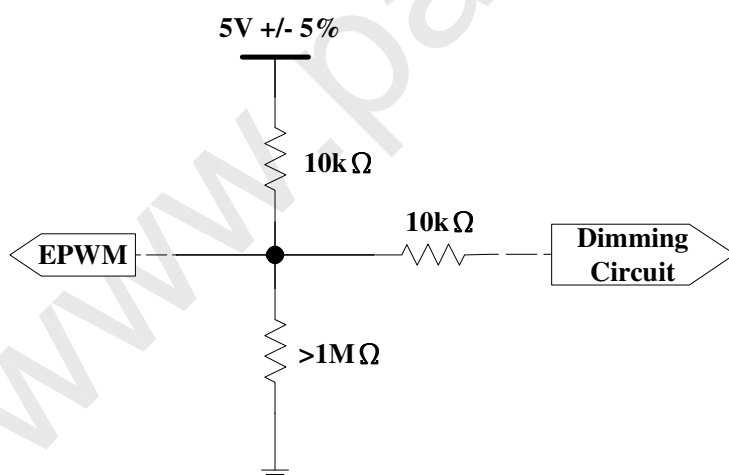
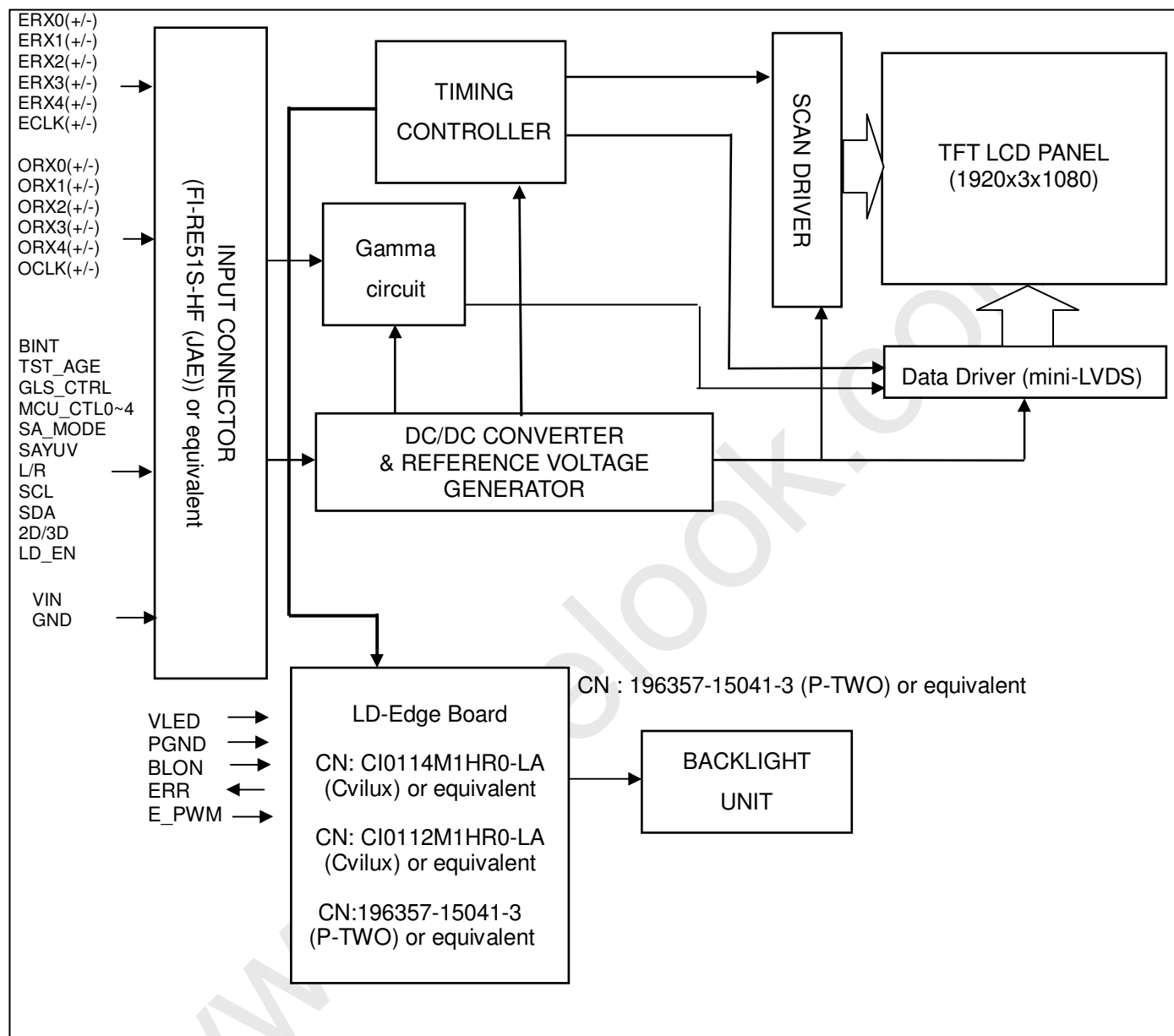


Fig. 2

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE





5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

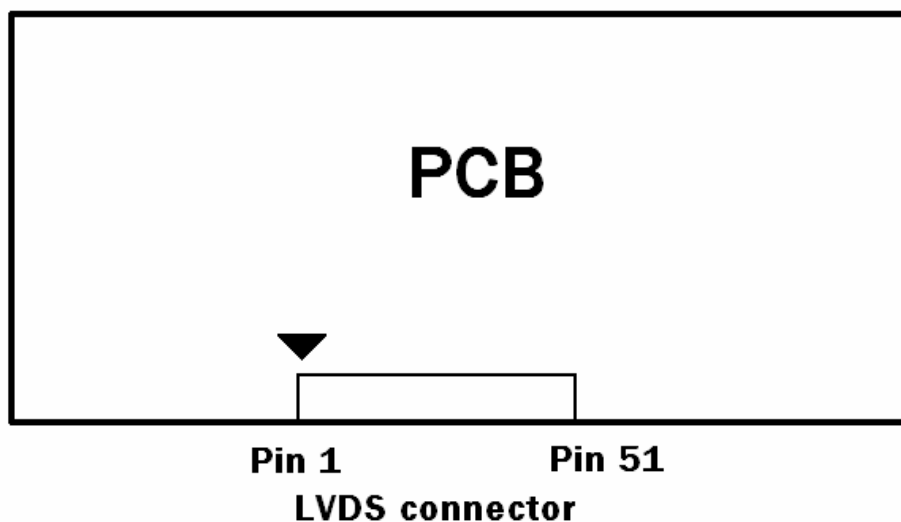
CNF1 Connector Part No.: P-TWO 187059-51221 or equivalent.

Pin	Name	Description	Note
1	BUS_SW	BUS_SW/BINT, pull-high as Auto-VCOM adjusting. (for Auto-VCOM)	(3)
2	SCL	I2C Serial Clock (for 3D format selection function)	
3	SDA	I2C Serial Data (for 3D format selection function)	
4	NC	No Connection	
5	L/R_O	Output signal for Left Right Glasses control	
6	GV_SEL	Graphic/Video mode selection	(3)
7	SELLVDS	Input signal for LVDS Data Format Selection	(4)
8	Blanking	Blanking enable	(5)
9	Bit select	8bit/10bit selection	(6)
10	MEMC demo	MEMC demo mode enable	(7)
11	GND	Ground	
12	ORX0-	1st pixel Negative LVDS differential data input. Channel 0	(1)
13	ORX0+	1st pixel Positive LVDS differential data input. Channel 0	
14	ORX1-	1st pixel Negative LVDS differential data input. Channel 1	
15	ORX1+	1st pixel Positive LVDS differential data input. Channel 1	
16	ORX2-	1st pixel Negative LVDS differential data input. Channel 2	(1)
17	ORX2+	1st pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	OCLK-	1st pixel Negative LVDS differential clock input.	
20	OCLK+	1st pixel Positive LVDS differential clock input	(1)
21	GND	Ground	
22	ORX3-	1st pixel Negative LVDS differential data input. Channel 3	(1)
23	ORX3+	1st pixel Positive LVDS differential data input. Channel 3	
24	ORX4-	1st pixel Negative LVDS differential data input. Channel 4	
25	ORX4+	1st pixel Positive LVDS differential data input. Channel 4	
26	2D/3D	Input signal for 2D/3D Mode Selection	(8)
27	L/R	Input signal for Left Right synchronous signal	
28	ERX0-	2nd pixel Negative LVDS differential data input. Channel 0	(1)
29	ERX0+	2nd pixel Positive LVDS differential data input. Channel 0	
30	ERX1-	2nd pixel Negative LVDS differential data input. Channel 1	
31	ERX1+	2nd pixel Positive LVDS differential data input. Channel 1	
32	ERX2-	2nd pixel Negative LVDS differential data input. Channel 2	
33	ERX2+	2nd pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	ECLK-	2nd pixel Negative LVDS differential clock input.	(1)
36	ECLK+	2nd pixel Positive LVDS differential clock input	
37	GND	Ground	
38	ERX3-	2nd pixel Negative LVDS differential data input. Channel 3	(1)
39	ERX3+	2nd pixel Positive LVDS differential data input. Channel 3	
40	ERX4-	2nd pixel Negative LVDS differential data input. Channel 4	
41	ERX4+	2nd pixel Positive LVDS differential data input. Channel 4	

42	LD_EN	Input signal for Local Dimming Enable	(9)
43	SCN_EN	Input signal for Scanning Enable	(10)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	NC	No Connection	
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

Note (1) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel

Note (2) LVDS connector pin order defined as follows



Note (3) G/V select. (Default : Graphic mode)

L= Connect to GND, H=Connect to +3.3V or Open

G/V select	Note
L	Video mode
H or Open	Graphic mode

Note (4) SELLVDS. (Default : VESA)

L= Connect to GND or Open, H=Connect to +3.3V

SELLVDS	Note
H or Open	VESA
L	JEIDA

Note (5) Blanking. (Default : Disable)

L= Connect to GND or Open, H=Connect to +3.3V

Blanking	Note
L or Open	Disable
H	Enable

Note (6) Bit select. (Default : 10bit)

L= Connect to GND or Open, H=Connect to +3.3V

Bit select	Note
L or Open	10bit
H	8bit

Note (7) MEMC demo. (Default : Disable)

L= Connect to GND or Open, H=Connect to +3.3V

MEMC demo	Note
L or Open	Disable
H	Enable

Note (8) 2D/3D. (Default : 2D)

L= Connect to GND or Open, H=Connect to +3.3V

2D/3D	Note
L or Open	2D mode
H	3D mode

Note (9) LD_EN. (Default : Disable)

L= Connect to GND or Open, H=Connect to +3.3V

LD_EN	Note
L or Open	Disable
H	Enable

Note (10) SCN_EN. (Default : Disable)

L= Connect to GND or Open, H=Connect to +3.3V

SCN_EN	Note
L or Open	Disable
H	Enable

5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN3、CN6: 196357-15041-3 (P-TWO)

Pin No.	Symbol	Feature
1	NC	No Connection
2	LED1	Negative of LED String
3	LED2	Negative of LED String
4	LED3	Negative of LED String
5	LED4	Negative of LED String
6	LED5	Negative of LED String
7	LED6	Negative of LED String
8	LED7	Negative of LED String
9	LED8	Negative of LED String
10	NC	No Connection
11	NC	No Connection
12	VCC_LED	Positive of LED String
13	VCC_LED	Positive of LED String
14	VCC_LED	Positive of LED String
15	VCC_LED	Positive of LED String

CN4、CN5: 196357-15041-3 (P-TWO)

Pin No.	Symbol	Feature
1	VCC_LED	Positive of LED String
2	VCC_LED	Positive of LED String
3	VCC_LED	Positive of LED String
4	VCC_LED	Positive of LED String
5	NC	No Connection
6	NC	No Connection
7	LED8	Negative of LED String
8	LED7	Negative of LED String
9	LED6	Negative of LED String
10	LED5	Negative of LED String
11	LED4	Negative of LED String
12	LED3	Negative of LED String
13	LED2	Negative of LED String
14	LED1	Negative of LED String
15	NC	Negative of LED String

5.3 CONVERTER UNIT

CN1: CI0114M1HR0-LA (Cvilux)

Pin №	Symbol	Feature
1	VLED	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	ERR	Normal (GND) Abnormal (Open collector)
12	BLON	BL ON/OFF
13	NC	NC
14	E_PWM	External PWM Control

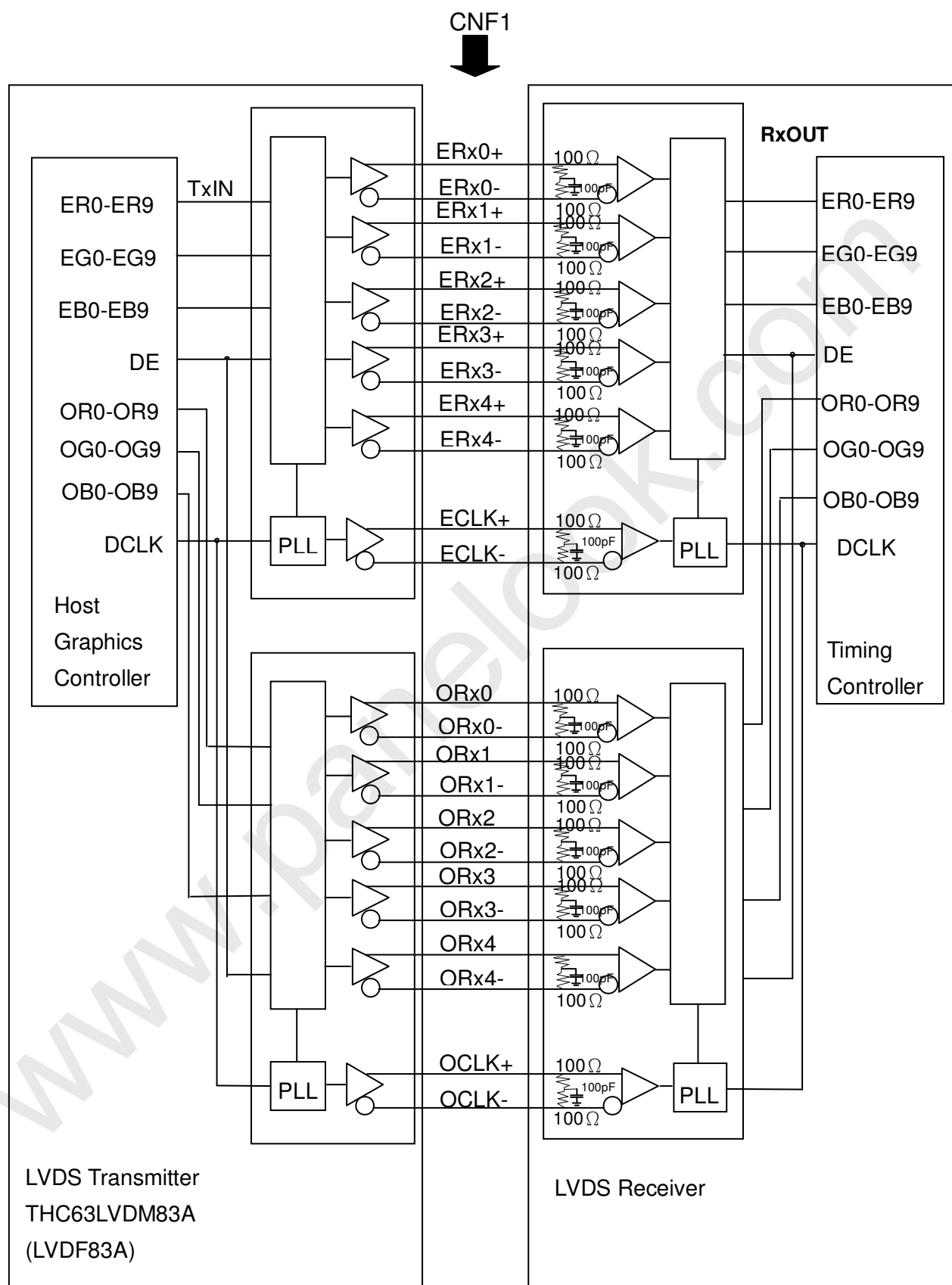
Notice: 1. If Pin14 is open, E_PWM is 100% duty.



CN2: CI0112M1HR0-LA (Cvilux)

Pin №	Symbol	Feature
1	VLED	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	NC	No Connection
12	NC	No Connection

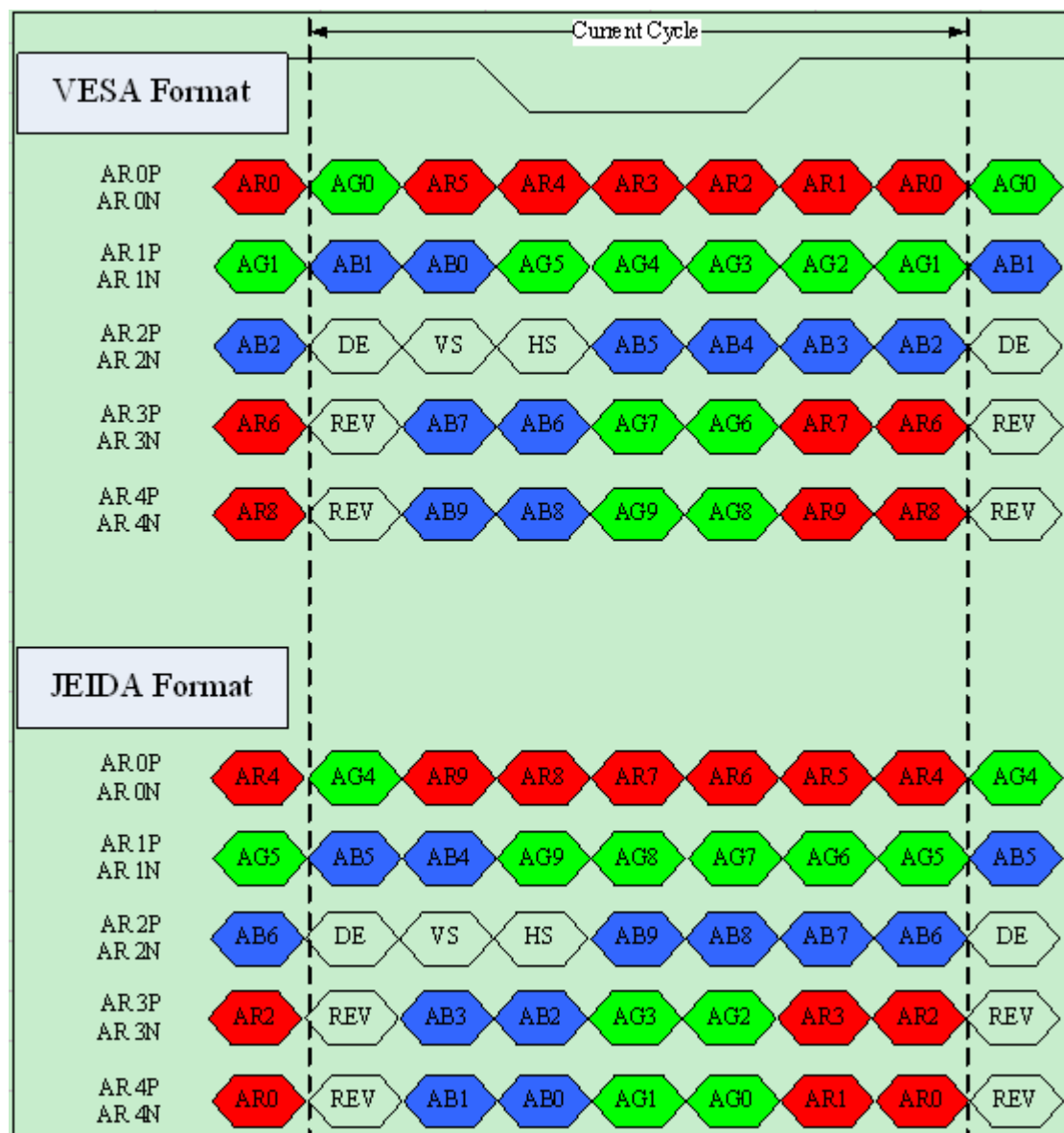
5.4 BLOCK DIAGRAM OF INTERFACE



5.5 LVDS INTERFACE

JEIDA Format : SELLVDS = L

VESA Format : SELLVDS = H or Open



R0~R9: Pixel R Data (9; MSB, 0; LSB)

G0~G9: Pixel G Data (9; MSB, 0; LSB)

B0~B9: Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																															
		Red										Green										Blue											
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0		
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 °C)

The input signal timing specifications are shown as the following table and timing diagram in the 2D mode.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	$F_{\text{clkin}} (=1/TC)$	68	75	79	MHz	
	Input cycle to cycle jitter	T_{rcl}	—	—	200	ps	(3)
	Spread spectrum modulation range	$F_{\text{clkin_mod}}$	$F_{\text{clkin}}-3\%$	—	$F_{\text{clkin}}+3\%$	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	—	—	150	KHz	(5)
LVDS Receiver Data	Receiver Skew Margin	T_{RSKM}	-400	—	400	ps	(6)

6.1.1 Timing spec for Frame Rate = 50Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r5}	47	50	53	Hz	
	3D mode		F_{r5}	50			Hz	
Vertical Active Display Term	2D Mode	Total	T_v	1115	1350	1395	Th	$T_v=T_{vd}+T_{vb}$
		Display	T_{vd}	1080			Th	—
		Blank	T_{vb}	35	270	315	Th	—
	3D Mdoe	Total	T_v	1350			Th	(6)
		Display	T_{vd}	1080			Th	(6)
		Blank	T_{vb}	270			Th	(6)
Horizontal Active Display Term	2D Mode	Total	T_h	1040	1100	1340	Tc	$T_h=T_{hd}+T_{hb}$
		Display	T_{hd}	960	960	960	Tc	—
		Blank	T_{hb}	80	140	380	Tc	—
	3D Mdoe	Total	T_h	1040	1100	1340	Tc	$T_h=T_{hd}+T_{hb}$
		Display	T_{hd}	960	960	960	Tc	—
		Blank	T_{hb}	80	140	380	Tc	—



6.1.2 Timing spec for Frame Rate = 60Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r6}	57	60	63	Hz	
	3D mode		F_{r6}	60			Hz	
Vertical Active Display Term	2D Mode	Total	T_v	1115	1125	1395	Th	$T_v = T_{vd} + T_{vb}$
		Display	T_{vd}	1080			Th	—
		Blank	T_{vb}	35	45	315	Th	—
	3D Mdoe	Total	T_v	1125			Th	(6)
		Display	T_{vd}	1080			Th	(6)
		Blank	T_{vb}	45			Th	(6)
Horizontal Active Display Term	2D Mode	Total	T_h	1040	1100	1340	Tc	$T_h = T_{hd} + T_{hb}$
		Display	T_{hd}	960	960	960	Tc	—
		Blank	T_{hb}	80	140	380	Tc	—
	3D Mdoe	Total	T_h	1040	1100	1340	Tc	$T_h = T_{hd} + T_{hb}$
		Display	T_{hd}	960	960	960	Tc	—
		Blank	T_{hb}	80	140	380	Tc	—

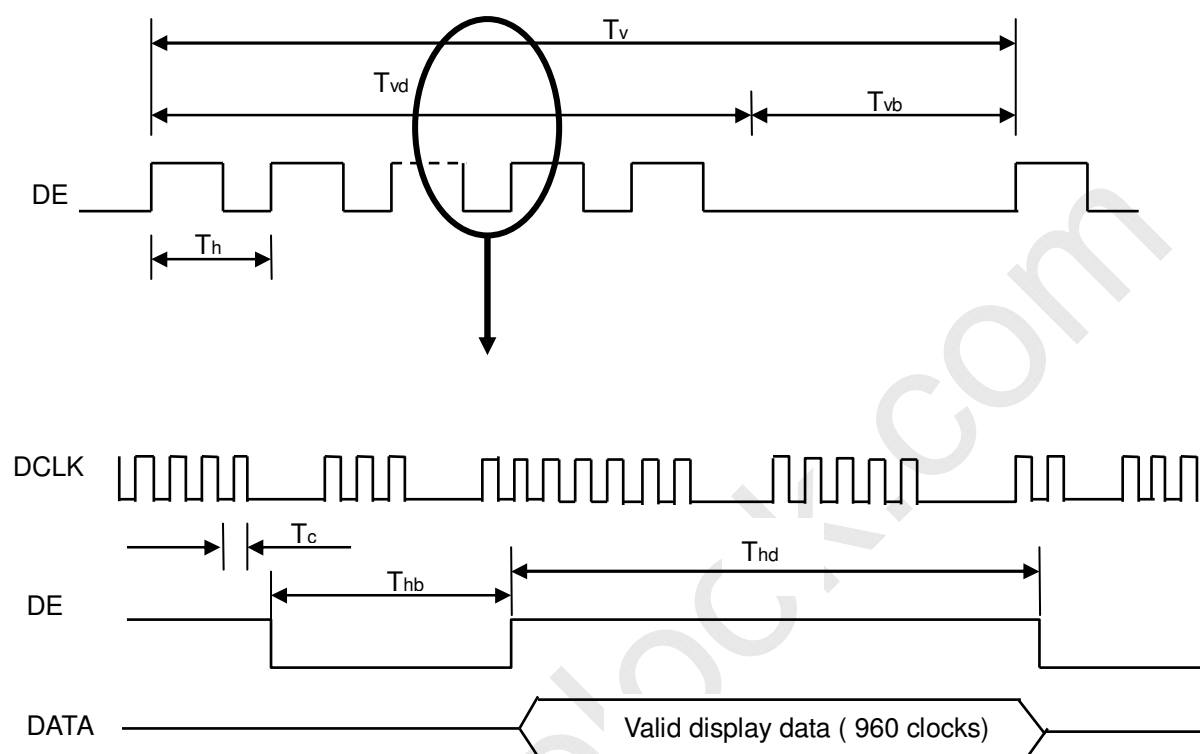
Note (1) Please make sure the range of pixel clock has follow the below equation :

$$F_{clkin}(\max) \geq F_{r6} \times T_v \times T_h$$

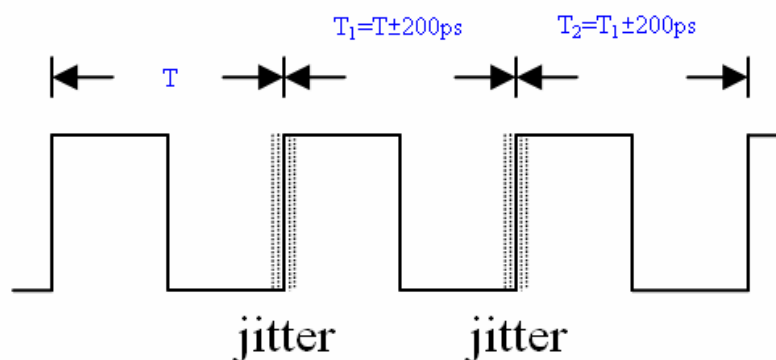
$$F_{r5} \times T_v \times T_h \geq F_{clkin}(\min)$$

Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below :

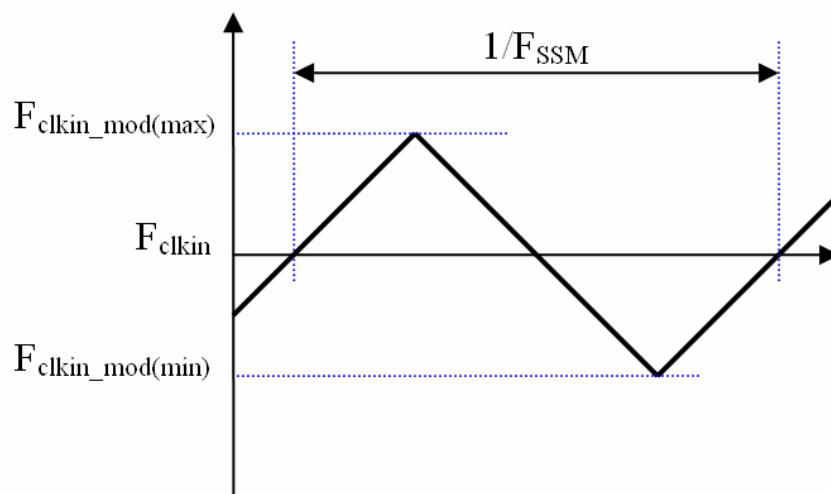
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. $Trcl = |T_1 - T_1|$



Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.

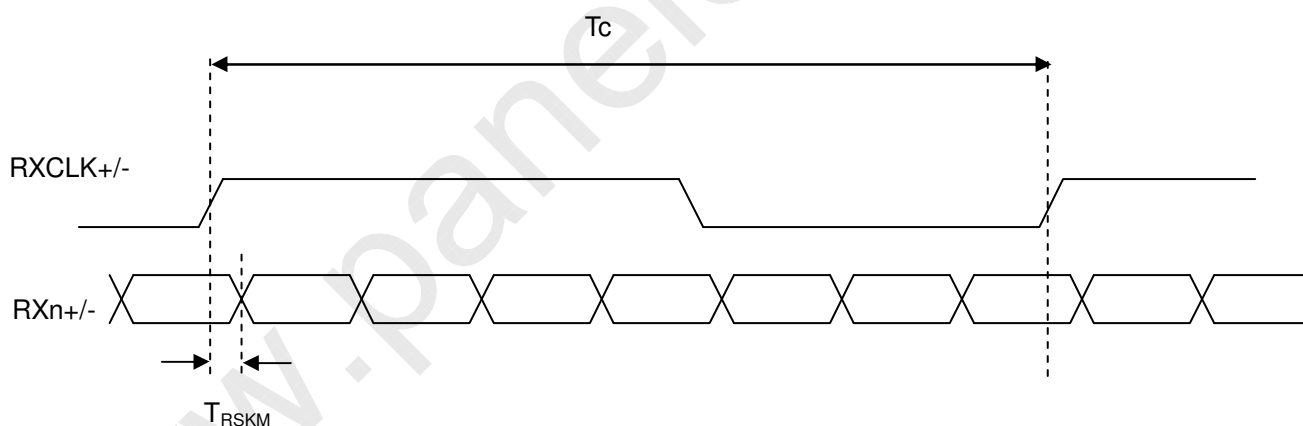


Note (5) Spread spectrum range should be constricted as below.

$$\text{SS Deviation (\%)} \times \text{SS Modulation Frequency (KHz)} \leq 150 (\% \cdot \text{KHz})$$

Note (6) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

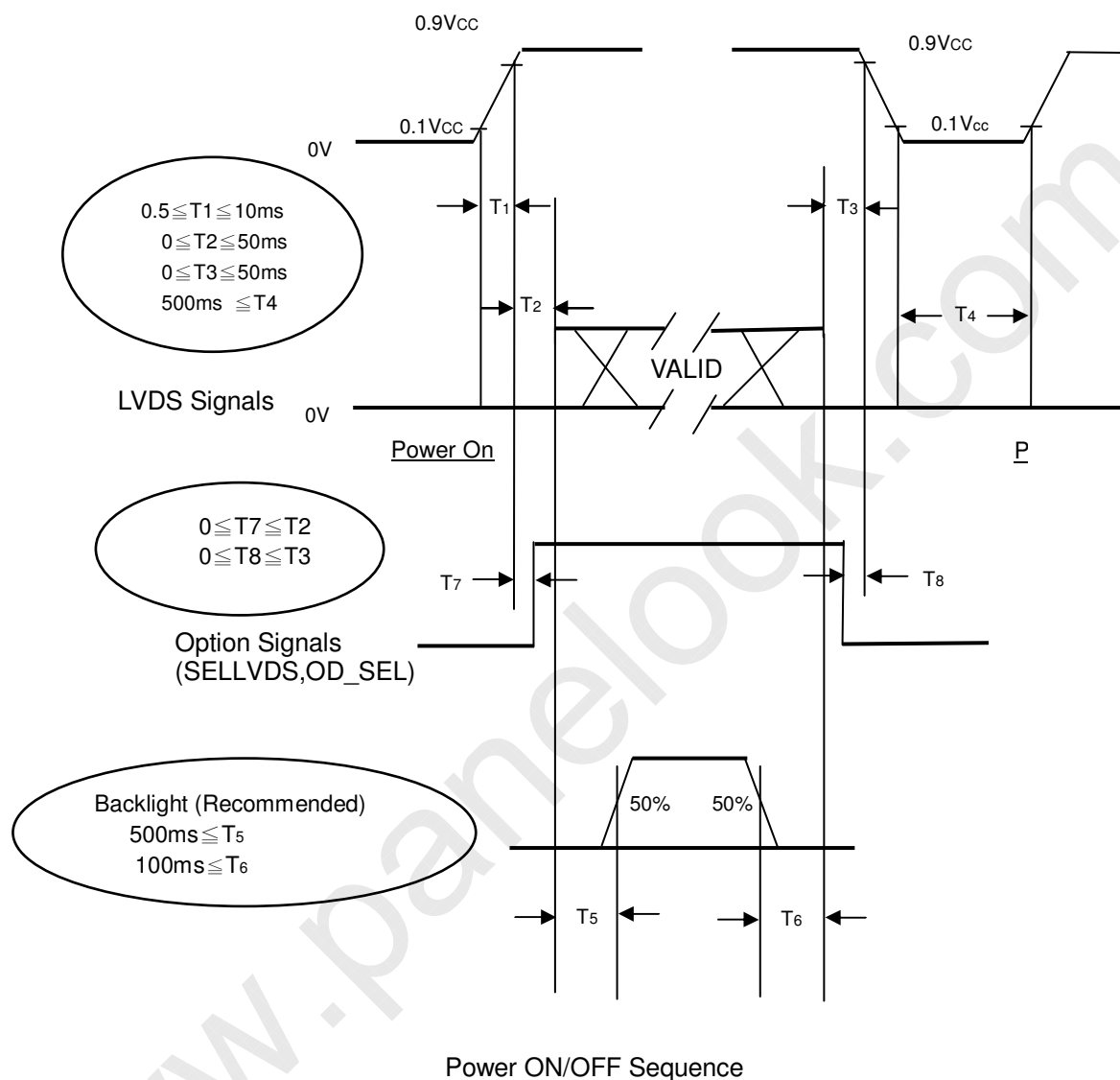
LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

($T_a = 25 \pm 2^\circ\text{C}$)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Note (1) The supply voltage of the external system for the module input should follow the definition of V_{CC} .

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of V_{CC} is in off level, please keep the level of input signals on the low or high impedance.

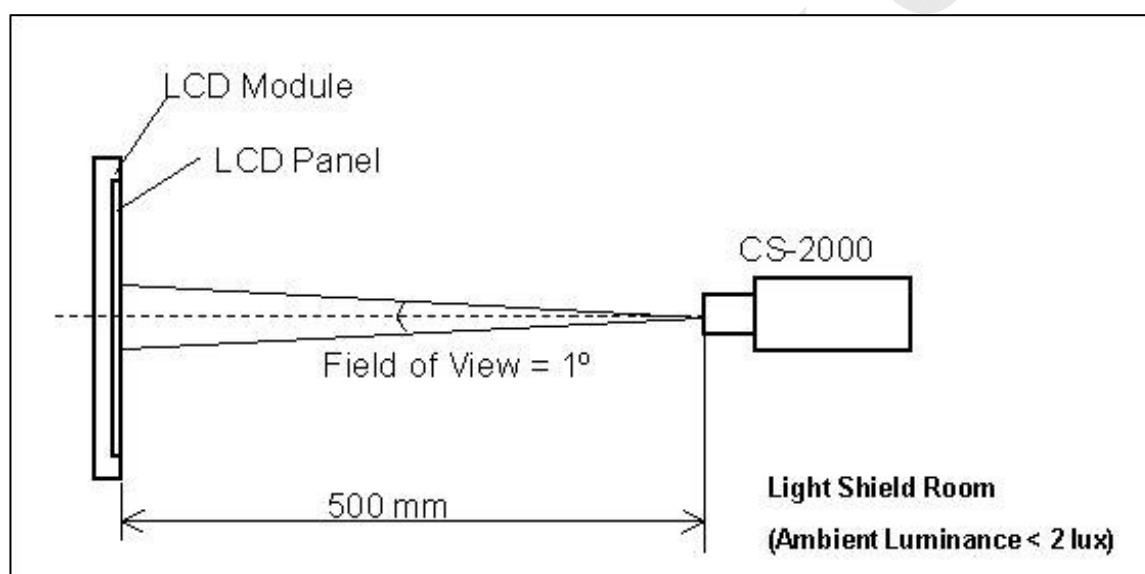
Note (4) $T4$ should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS**7.1 TEST CONDITIONS**

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	12±1.2	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	I _L	150±9	mA

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



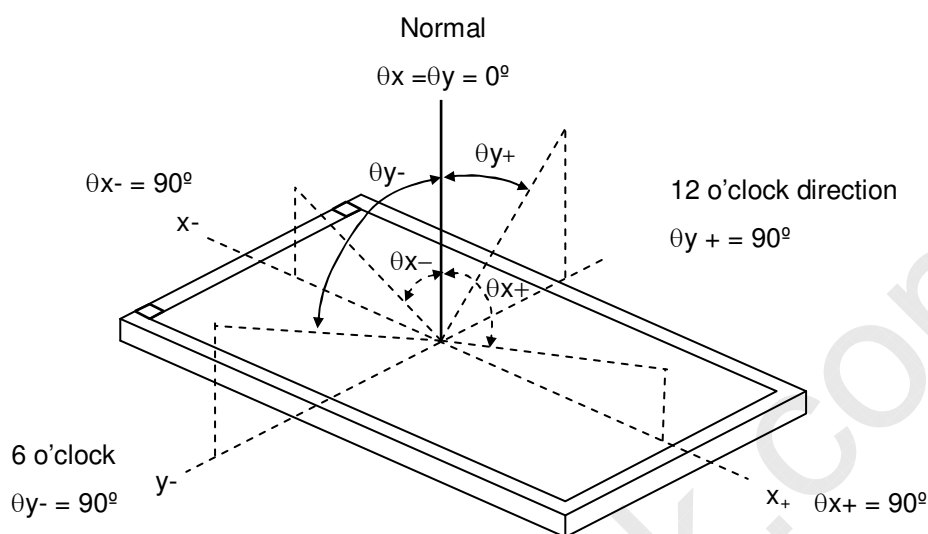
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol		Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing angle at normal direction	3000	5000	-	-	(2)
Response Time (VA)		Gray to gray			-	6.5	-	ms	(3)
Center Luminance of White		L _c	2D		300	330	-	cd/m ²	(4)
			3D		-	45	-	cd/m ²	(8)
White Variation		δW			-	-	1.3	-	(6)
Cross Talk		CT	2D		-	-	4	%	(5)
			3D-W		-	4	-	%	(8)
			3D-D		-	11	-	%	(8)
Color Chromaticity	Red	Rx			Typ. -0.03	0.630	Typ. +0.03	-	-
		Ry				0.336		-	
	Green	Gx				0.298		-	
		Gy				0.602		-	
	Blue	Bx				0.151		-	
		By				0.057		-	
	White	Wx				0.280		-	
		Wy				0.290		-	
	Correlated color temperature					-		10500	
	Color Gamut		C.G.		-	70	-	%	NTS C
Viewing Angle	Horizontal	θ_{x+}		CR $\geq$ 20 (VA)	80	88	-	Deg.	(1)
		θ_{x-}			80	88	-		
	Vertical	θ_{y+}			80	88	-		
		θ_{y-}			80	88	-		
Transmission direction of the up polarizer		Φ_{up-P}		-	-	90	-	Deg.	(7)
slow axis of the QWP		Φ_{up-Q}		-	-	135	-	Deg.	(7)

Note (1) Definition of Viewing Angle (θ_x , θ_y) :

Viewing angles are measured by Autronic Conoscope Cono-80



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

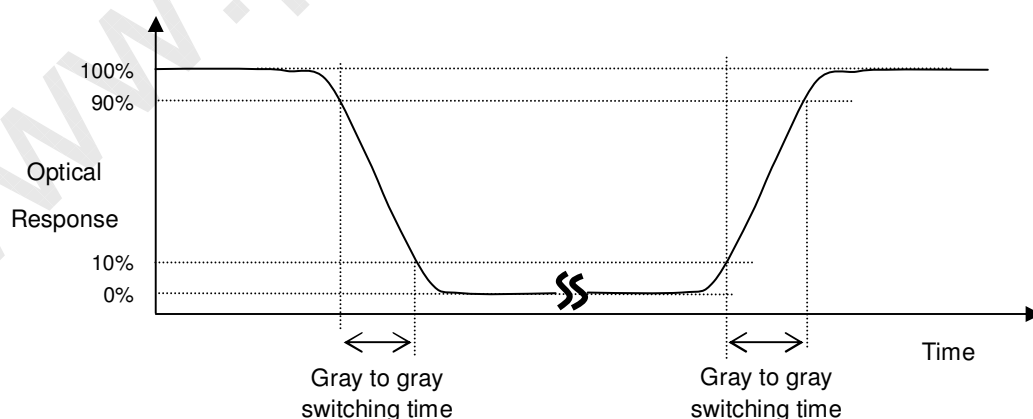
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

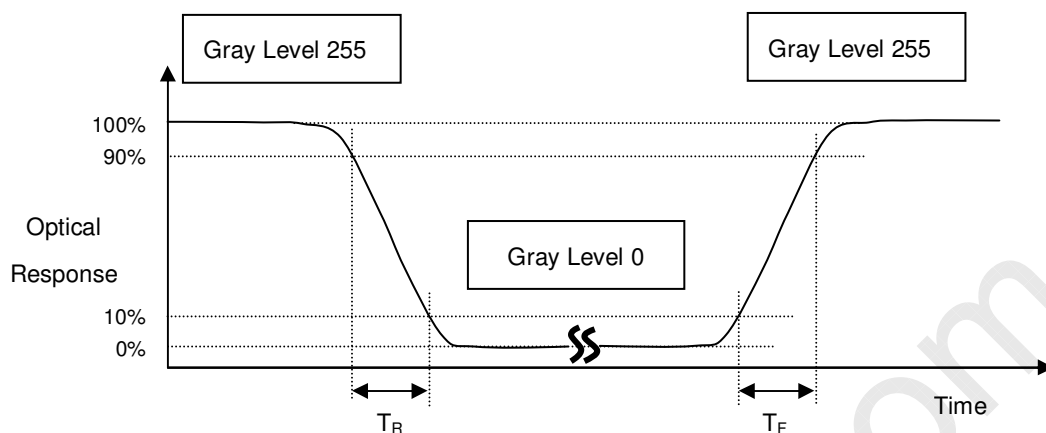
Note (3) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 32, 64, 96, 128, 160, 192, 224 and 256

Gray to gray average time means the average switching time of gray level 0, 32, 64, 96, 128, 160, 192, 224 and 256 to each other.

Note (3) Definition of Response Time (T_R , T_F):



Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L(5)$, where $L(X)$ is corresponding to the luminance of the point X at the figure in Note (6)..

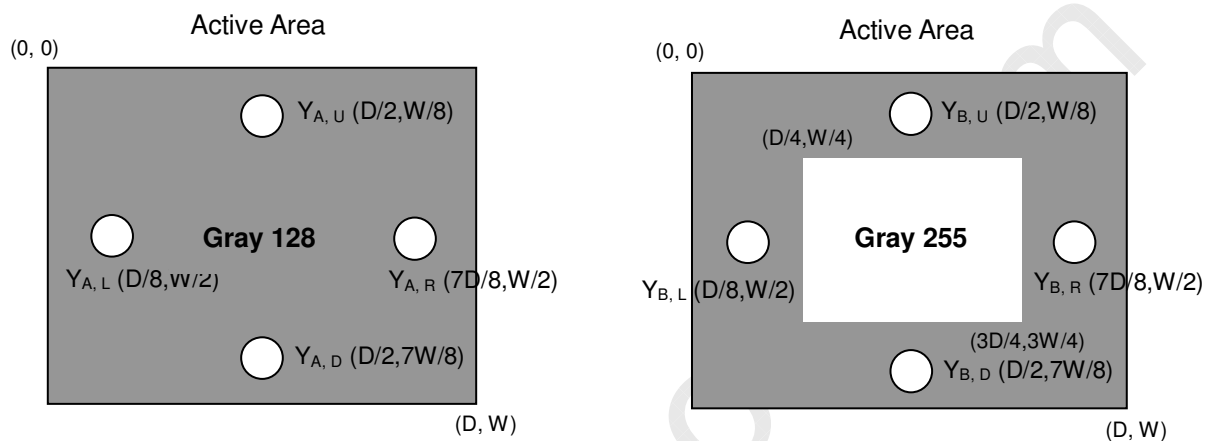
Note (5) Definition of Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

Y_A = Luminance of measured location without gray level 255 pattern (cd/m²)

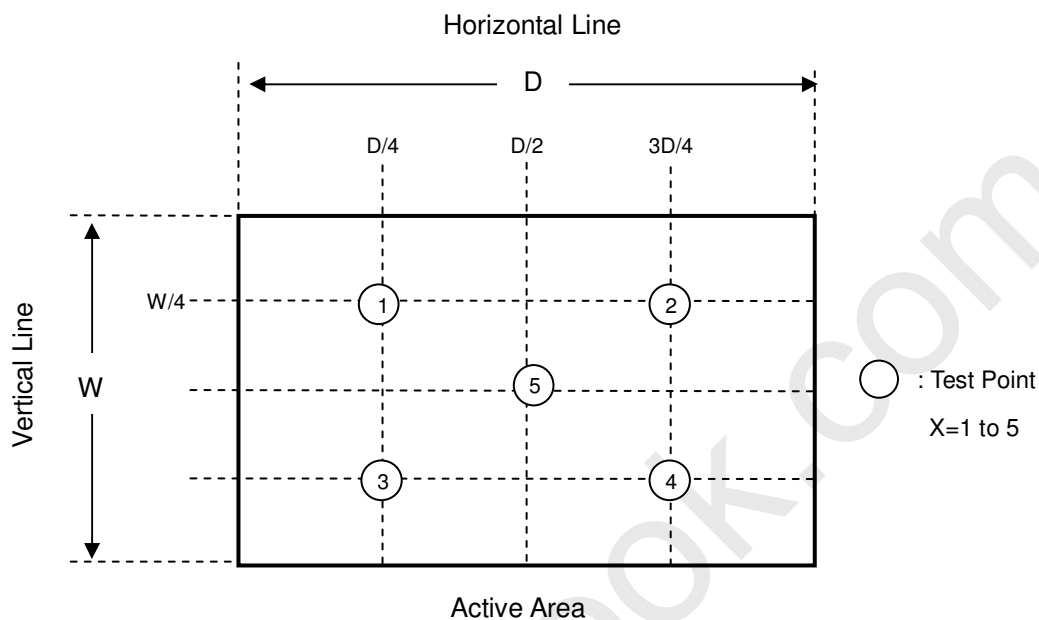
Y_B = Luminance of measured location with gray level 255 pattern (cd/m²)



Note (6) Definition of White Variation (δW):

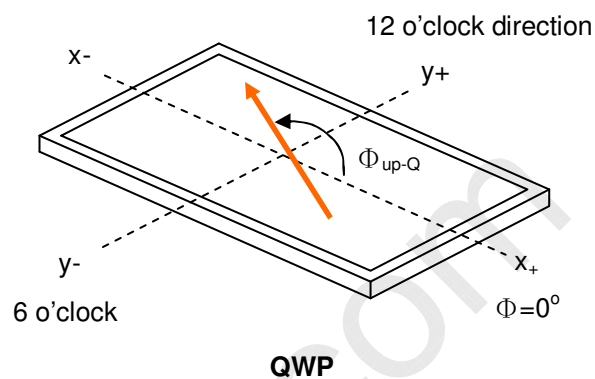
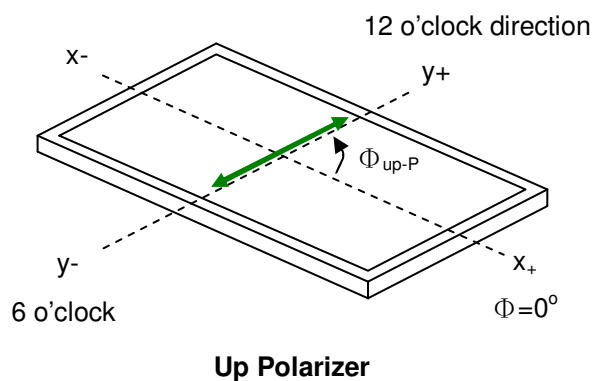
Measure the luminance of gray level 255 at 5 points

$$\delta W = \text{Maximum [L (1), L (2), L (3), L (4), L (5)]} / \text{Minimum [L (1), L (2), L (3), L (4), L (5)]}$$

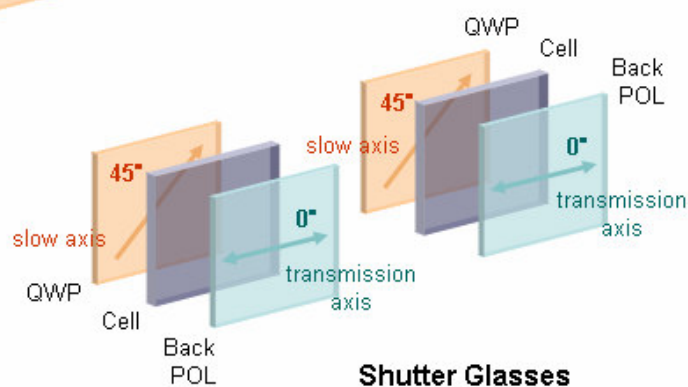
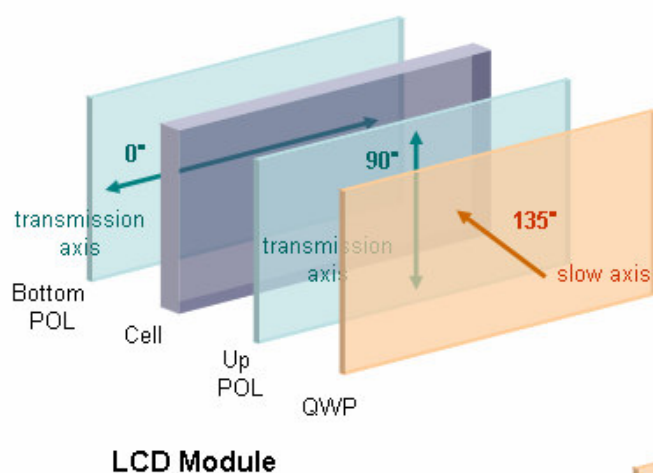


Note (7) This is a reference for designing the shutter glasses of 3D application.

Definition of the transmission direction of the up polarizer (Φ_{up-P}) and the slow axis of QWP (Φ_{up-Q}) on LCD Module:



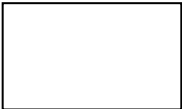
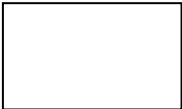
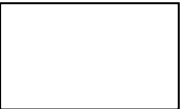
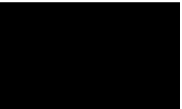
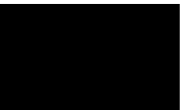
The slow axis of the QWP on shutter glasses should be perpendicular to the QWP on LCD Module to get better 3D performance.



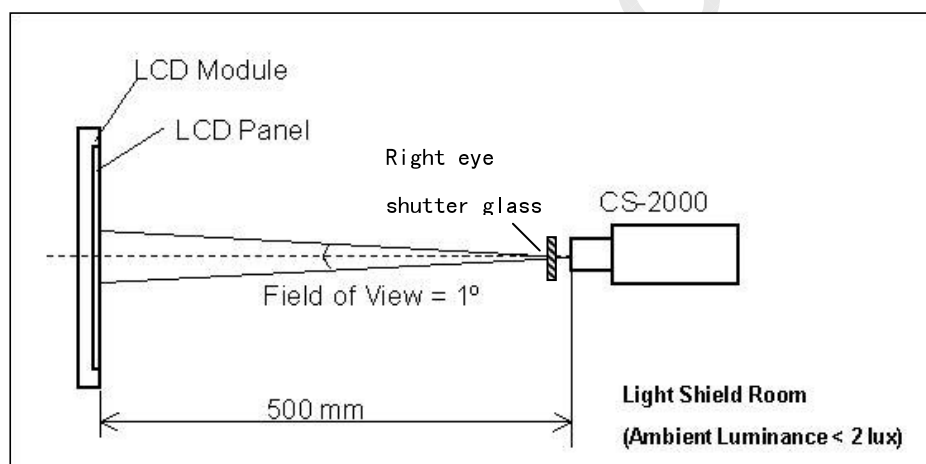
Note (8) Definition of the 3D mode performance (measured under 3D mode, use CMI's shutter glass):

a. Test pattern

Left eye image and right eye image are displayed alternated

		WW Left eye image: W255; Right eye image: W255
		WB Left eye image: W255; Right eye image: W0
		BW Left eye image: W0; Right eye image: W255
		BB Left eye image: W0; Right eye image: W0

b. Measurement setup



Shutter glasses are well controlled under suitable timing, and measure the luminance of the center point of the panel through the right eye glass. The transmittance of the glass should be larger than 40.0% under 3D mode operation.

The luminance of the test pattern "WW", denoted $L(WW)$; the luminance of the test pattern "WB", denoted $L(WB)$; the luminance of the test pattern "BW", denoted $L(BW)$; the luminance of the test pattern "BB", denoted $L(BB)$

c. Definition of the Center Luminance of White, L_c (3D) : $L(WW)$

d. Definition of the 3D mode white crosstalk, CT (3D-W) : $CT(3D-W) \equiv \frac{L(WB) - L(BB)}{L(WW) - L(BB)}$

Definition of the 3D mode dark crosstalk, CT (3D-D) : $CT(3D-D) \equiv \frac{L(WW) - L(BW)}{L(WW) - L(BB)}$

8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

- [1] Do not apply rough force such as bending or twisting to the module during assembly.
- [2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- [3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.
- [4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- [5] Do not plug in or pull out the I/F connector while the module is in operation.
- [6] Do not disassemble the module.
- [7] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- [8] Moisture can easily penetrate into LCD module and may cause the damage during operation.
- [9] When storing modules as spares for a long time, the following precaution is necessary.
 - [9.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
 - [9.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

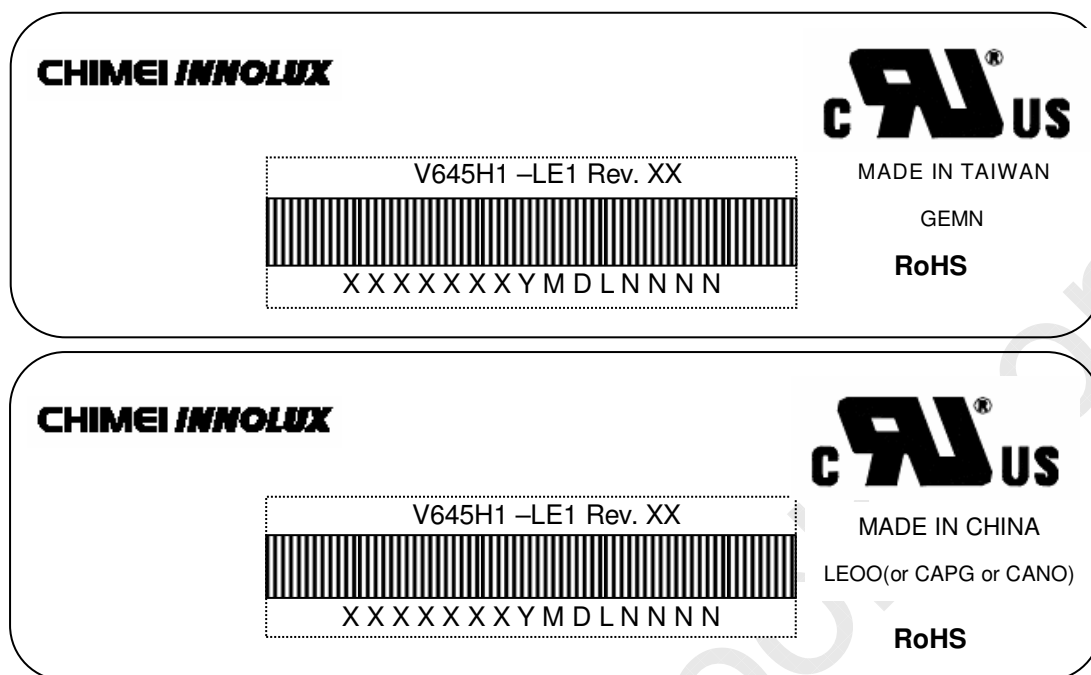
8.2 SAFETY PRECAUTIONS

- [1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.
- [2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- [3] After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMI MODULE LABEL

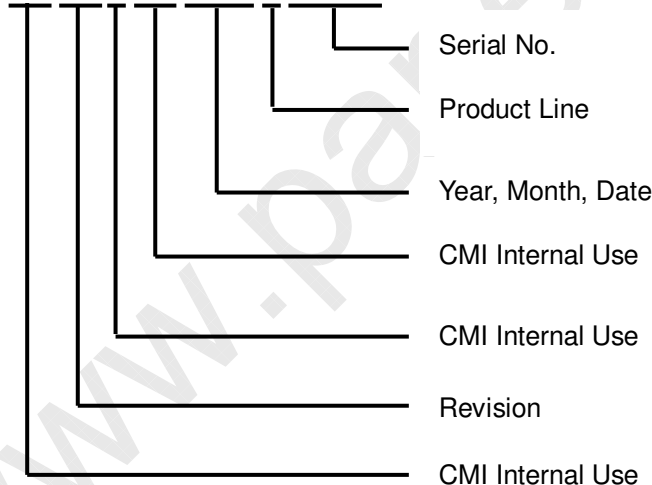
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V645H1-LE1

Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.

Serial ID: XXXXXYYMDLNNNN



Serial ID includes the information as below:

Manufactured Date:

Year : 2001=1, 2002=2, 2003=3, 2004=4...2010=0, 2011=1, 2012=2...

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I, O, and U.

Revision Code : Cover all the change

Serial No. : Manufacturing sequence of product

Product Line : 1 → Line1, 2 → Line 2, ...etc.

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

- (1) 15 LCD TV modules / 1 Box
- (2) Box dimensions : 1637(L)x1128(W)x955(H)mm
- (3) Weight : Approx. 480Kg(15 modules per carton)

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method

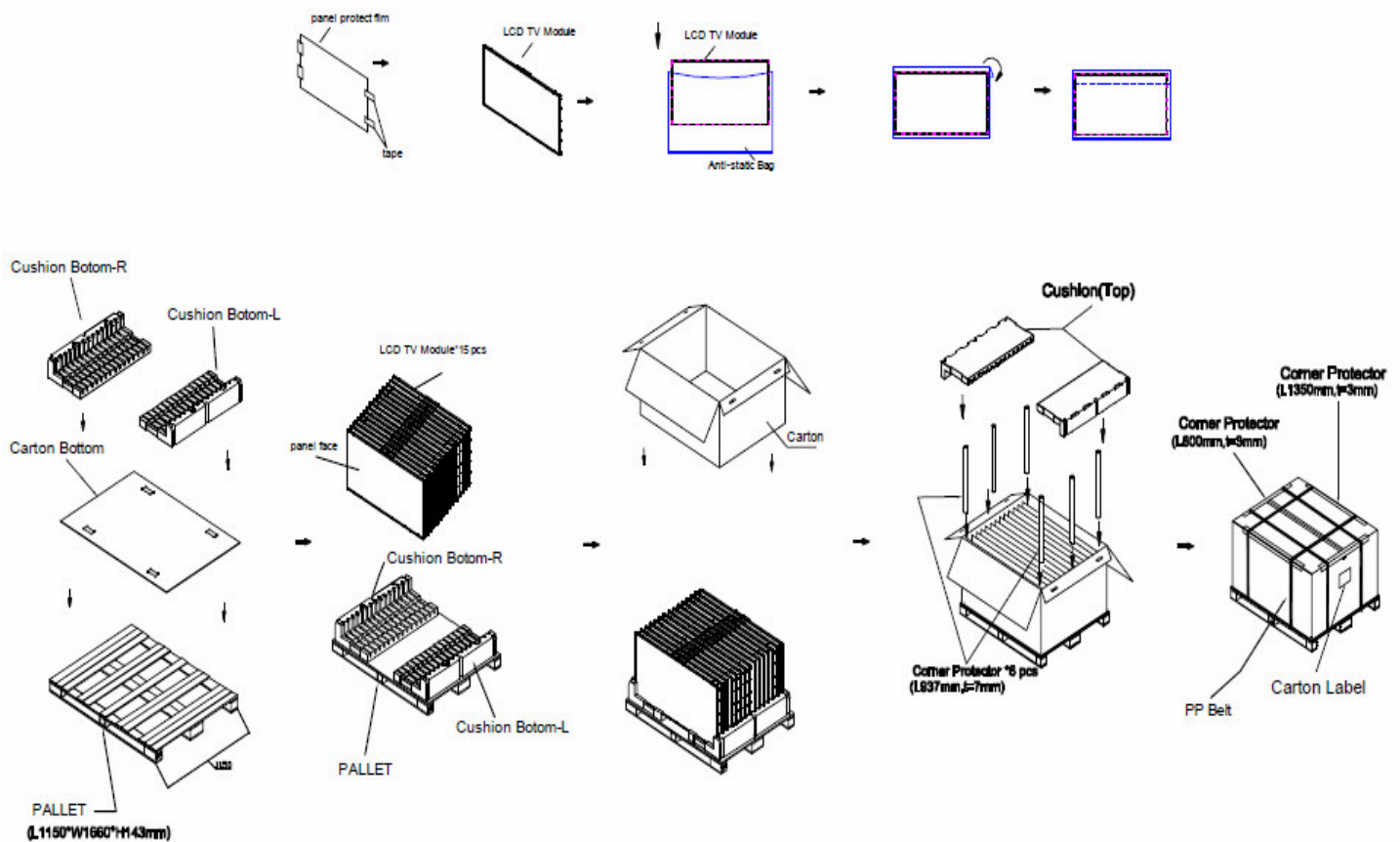


Figure 10-1 packing method

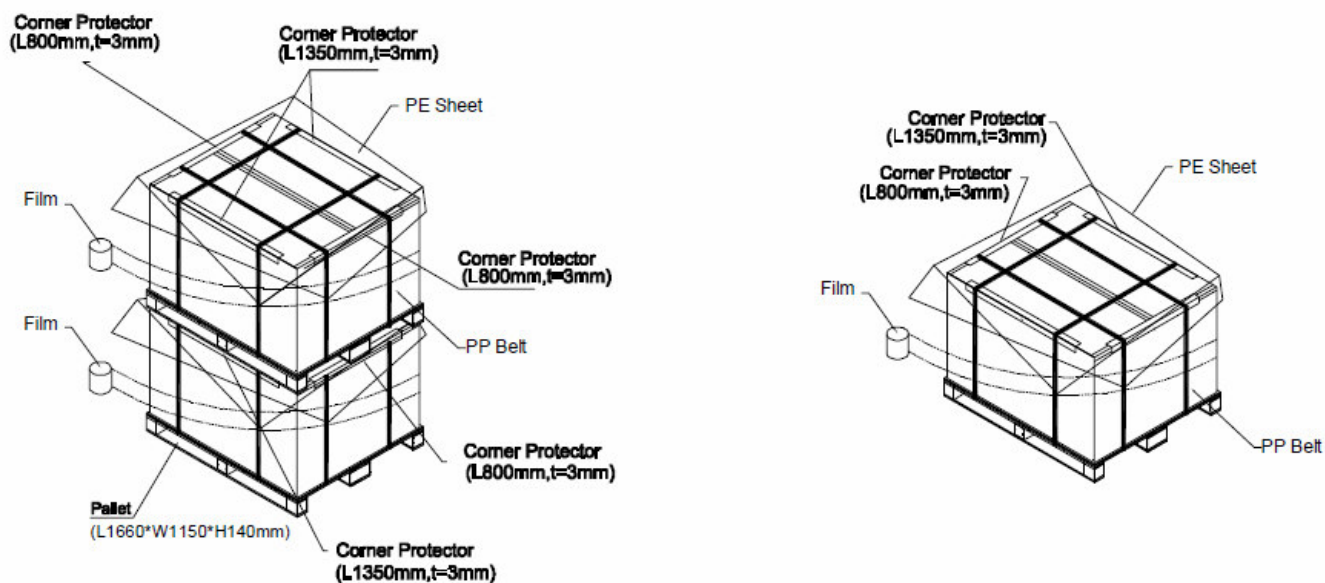
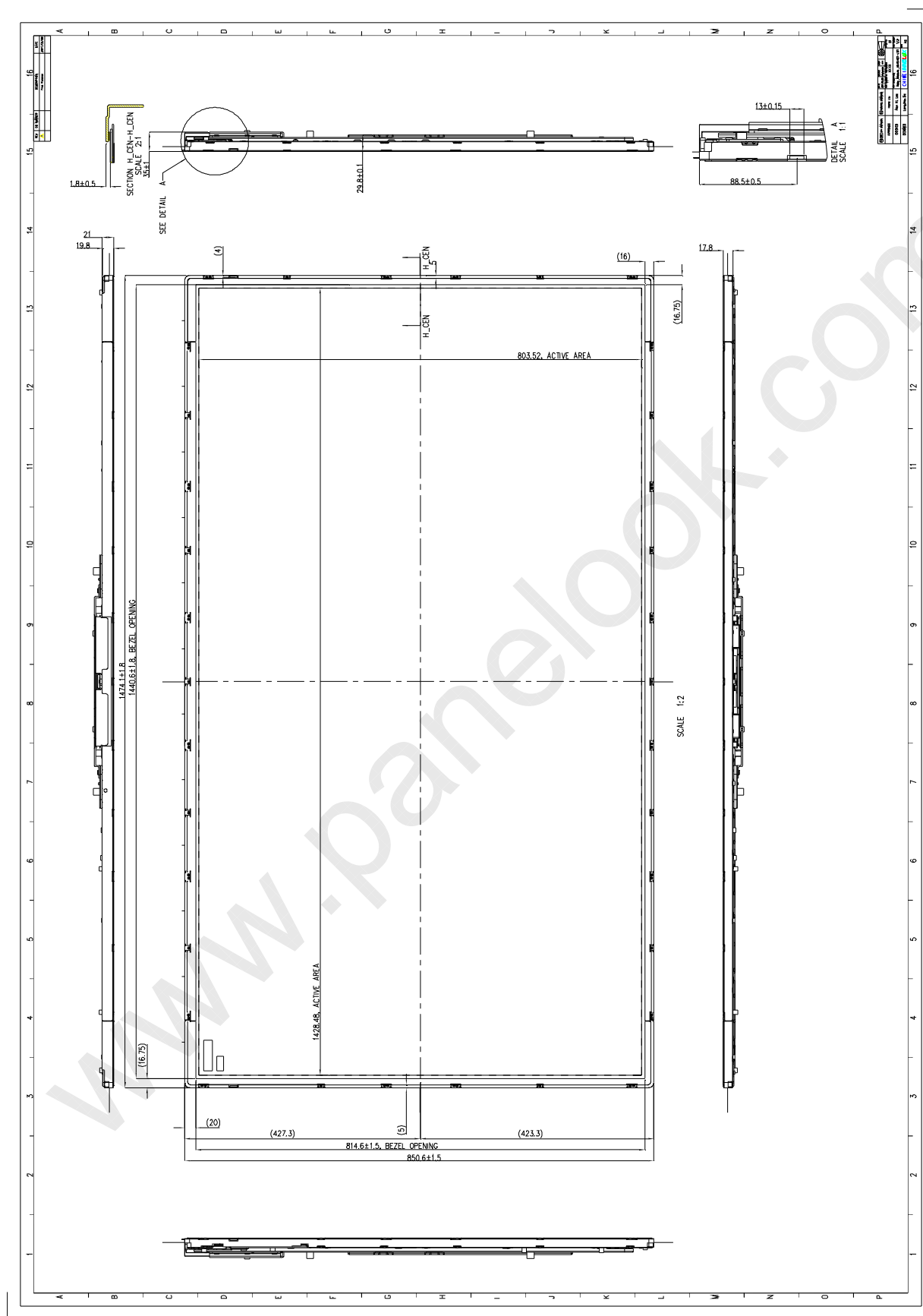
**Sea & Land Transportation****Air Transportation**

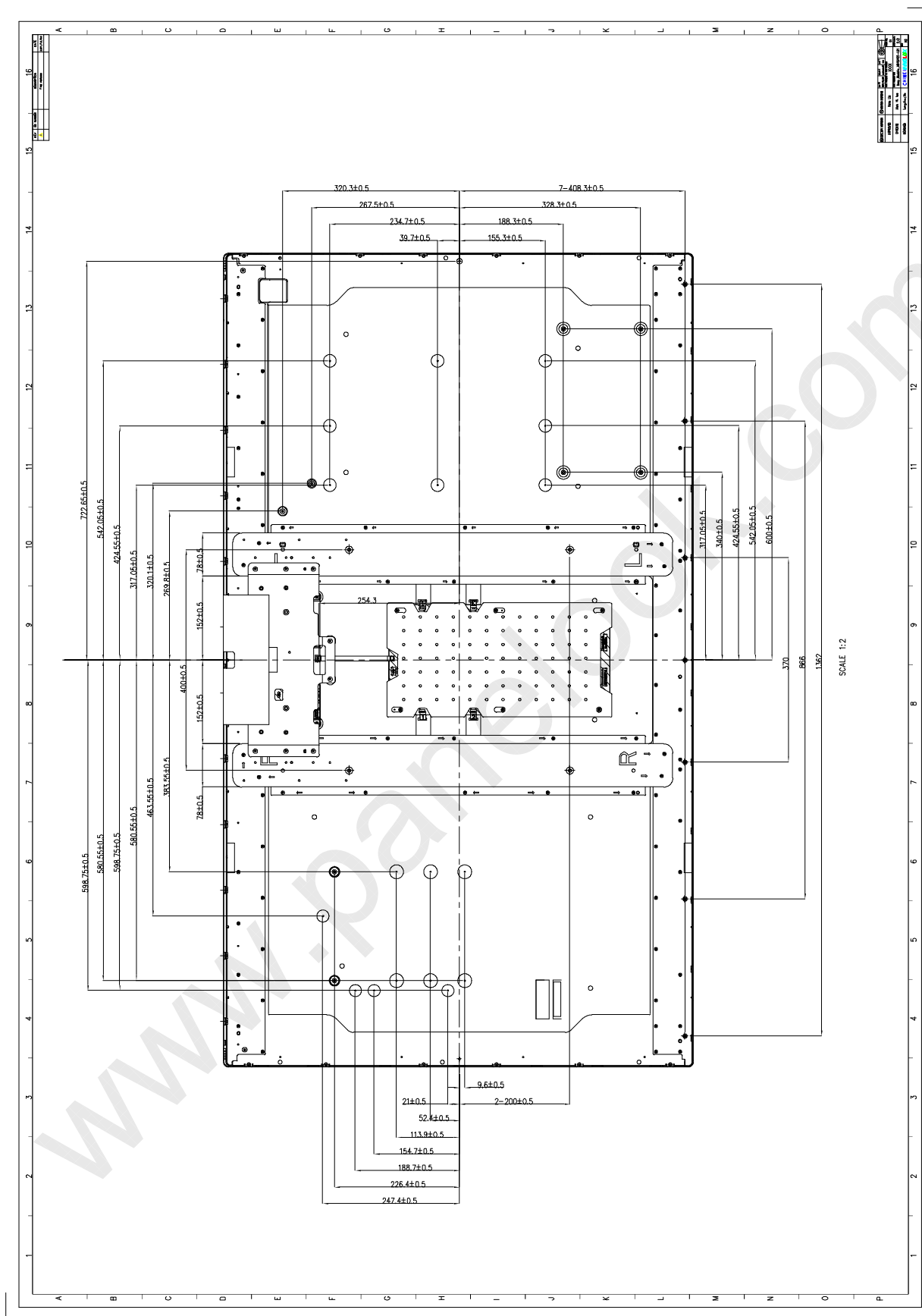
Figure 10-2 packing method

**11. MECHANICAL CHARACTERISTIC**



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PRODUCT SPECIFICATION



Appendix – TWO Wire BUS INTRODUCTION

A.1 PIN ASSIGNMENT

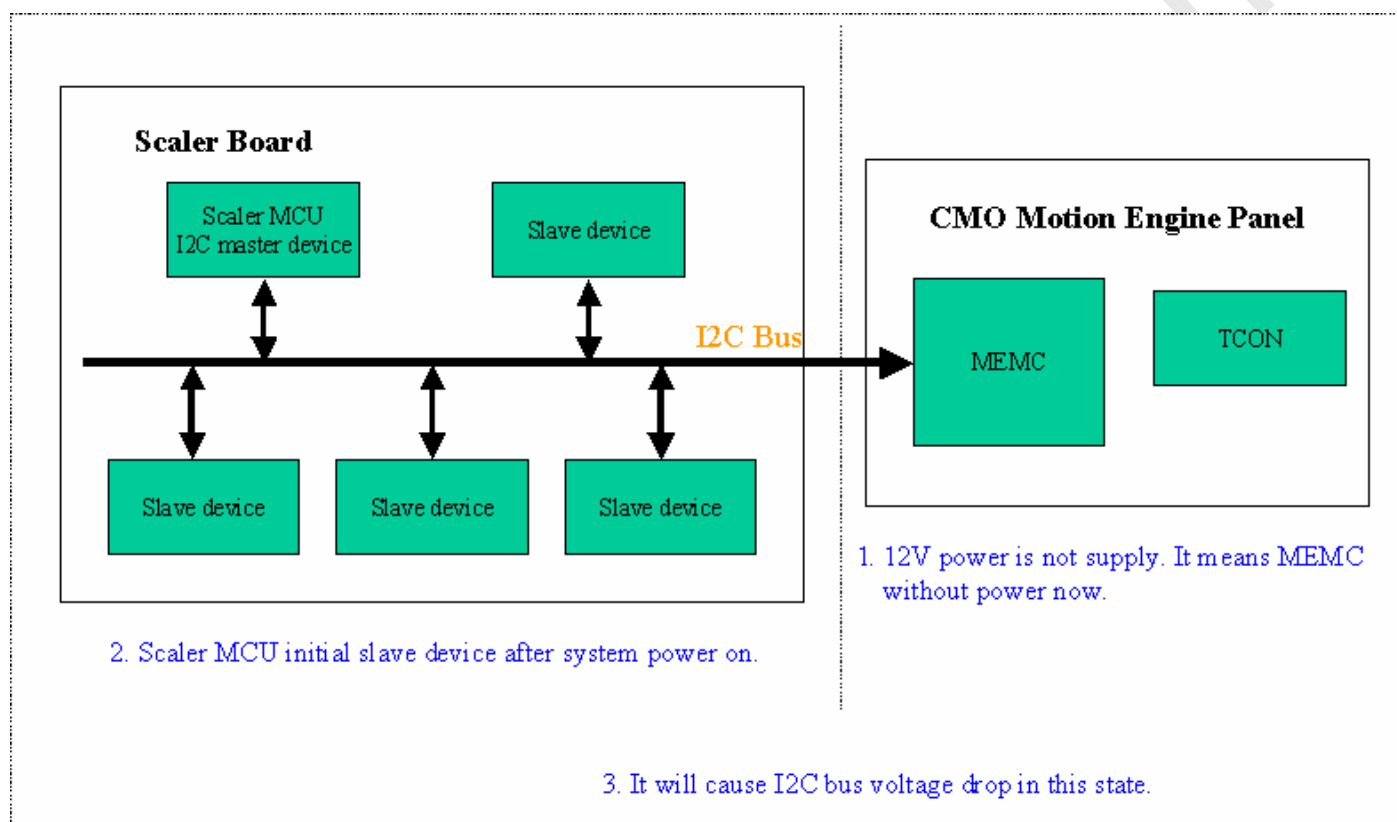
51pins LVDS connector

Pin2: SCL

Pin3: SDA

A.2 I2C BUS APPLICATION NOTE

I2C bus: (The I2C bus must for MEMC only or prevent the I2C bus voltage drop down in initial state)



A.3 TWO WIRE BUS DEVICE ADDRESS

Two wire device address: default is 0x40, 1 byte

Two wire command: the range is 0x00 to 0xFF, 1 byte, see the two wire command table.

Two wire bus format:

Device Address : 0X40 default							
D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	0	0	W

W	Write : 0
S	TWI-Bus Star condition from master
A	TWI-Bus Acknowledge bit from master
P	TWI-Bus Stop condition from master
Data	TWI-Bus Data from master

A.4 TWO WAY TO CONTROL THE TWO WIRE BUS

There are two options to control the two wires bus command.

Two wire bus 6 bytes format

TWI BUS 6 BYTES FORMAT														
Wire Operation														
	MSB		LSB		MSB		LSB		MSB		LSB		MSB	
S	Device Addr		0	A	Command		A	1st Data	A	2nd Data	A	3rd Data	A	4th Data
1 bit	7 bit		W	1 bit	8 bit		1 bit	8 bit	1 bit	8 bit	1 bit	8 bit	1 bit	8 bit

Two wire bus 3 bytes format

TWI BUS 3 BYTES FORMAT										
Wire Operation										
	MSB		LSB		MSB		LSB		MSB	
S	Device Addr		0	A	Command		A	1st Data	A	P
1 bit	7 bit		W	1 bit	8 bit		1 bit	8 bit	1 bit	1 bit

Note:

A transmission basically consists of a START condition, a SLA+R/W, one or more data packets and a STOP condition. An empty message, consisting of a START followed by a STOP condition, is illegal. Note that the wired-ANDing of the SCL line can be used to implement handshaking between the master and the slave. The slave can extend the SCL low period by pulling the SCL line low. This is useful if the clock speed set up by the master is too fast for the slave, or the slave needs extra time for processing between the data transmissions. The slave extending the SCL low period will not affect the SCL high period, which is determined by the master. As a consequence, the slave can reduce the TWI data transfer speed by prolonging the SCL duty cycle.

A.5 TWO WIRE BUS COMMAND TABLE

There is two wire bus command table.

I. OSD Protection

Command		Access Mode	Description	Remark
All OSD Protection	0x00	W	All OSD Protection	Note(10)
OSD1_Start_Protection	0x01	W	OSD1_Start_Protection	Note(11)
OSD2_Start_Protection	0x02	W	OSD2_Start_Protection	
OSD3_Start_Protection	0x03	W	OSD3_Start_Protection	
OSD4_Start_Protection	0x04	W	OSD4_Start_Protection	
OSD1_Size_Protection	0x05	W	OSD1_Size_Protection	Note(12)
OSD2_Size_Protection	0x06	W	OSD2_Size_Protection	
OSD3_Size_Protection	0x07	W	OSD3_Size_Protection	
OSD4_Size_Protection	0x08	W	OSD4_Size_Protection	

Note(10)

AllOSD Protection : 0x00										
1 Byte Data Length										
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D4	Unused
	Unusaed				OSDx				D3	OSD4 flag 1 : On ; 0 : Off
									D2	OSD3 flag 1 : On ; 0 : Off
									D1	OSD2 flag 1 : On ; 0 : Off
									D0	OSD1 flag 1 : On ; 0 : Off

Note(11)

OSD1_Start_Protection : 0x01										
OSD2_Start_Protection : 0x02										
OSD3_Start_Protection : 0x03										
OSD4_Start_Protection : 0x04										
4 Bytes Data Length										
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D27	Unused
	Unused								D26~D16	OSDx Left Position
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D15~D11	Unused
	OSD Left								D10~D0	OSDx Top Position
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8	Left Position Max : 1919 Top Position Max : 1079	
	Unused									
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0		
	OSD Top									

Note(12)

OSD1_Size_Protection : 0x05																					
OSD2_Size_Protection : 0x06																					
OSD3_Size_Protection : 0x07																					
OSD4_Size_Protection : 0x08																					
4 Bytes Data Length																					
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	<table><tr><td>D31~D27</td><td>Unused</td></tr><tr><td>D26~D16</td><td>OSDx Length</td></tr><tr><td>D15~D11</td><td>Unused</td></tr><tr><td>D10~D0</td><td>OSDx Width</td></tr><tr><td colspan="2">Length Max : 1919</td></tr><tr><td colspan="2">Width Max : 1079</td></tr></table>	D31~D27	Unused	D26~D16	OSDx Length	D15~D11	Unused	D10~D0	OSDx Width	Length Max : 1919		Width Max : 1079	
D31~D27	Unused																				
D26~D16	OSDx Length																				
D15~D11	Unused																				
D10~D0	OSDx Width																				
Length Max : 1919																					
Width Max : 1079																					
	Unused																				
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16													
	OSD Length																				
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8													
	Unused																				
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0													
	OSD Width																				

II. 2D Function

Command	Access Mode	Description	Remark
Demo Window	0x09	W	Demo Window on/off
MEMC Level	0x0A	W	MEMC Level tuning
GV Mode	0x0B	W	GV Mode select
Blanking	0x0C	W	Blanking on/off
BU LD	0x0D	W	Backlight Local Dimming on/off
LVDS	0x0E	W	LVDS select
Auto Blanking	0x0F	W	Auto Blanking

Note(13)

Demo Window : 0x09											
1 Byte Data Length											
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0		D7~D1	Unused
	Unused									D0	
										Demo Window 1 : on ; 0 : off	

Note(14)

MEMC Level : 0x0A											
1 Byte Data Length											
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D4	Unused	
	Unused				MEMC Level				D3~D0	MEMC Level 0~F	
									0 : Off		
									3 : Weak		
									8 : Normal		
									D : Strong		

MEMC Level (Default Normal)

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Date : 05 October, 2011

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Note(15)

GV Mode : 0x0B											
1 Byte Data Length											
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D1	Unused	
	Unused								D0	1 : Graphic ; 0 : Video	

GV Mode (Default Graphic Mode)

Note(16)

Blanking : 0x0C											
1 Byte Data Length											
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D1	Unused	
	Unused								D0	Blanking 1 : On ; 0 : Off	

Blanking (Default Off)

Note(17)

BU LD : 0x0D											
1 Byte Data Length											
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D1	Unused	
	Unused								D0	BU LD 1 : On ; 0 : Off	

BU LD (Default Off)

Note(18)

LVDS : 0x0E												
1 Byte Data Length												
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D1	Unused		
	Unused								D0	LVDS 1 : JEIDA ; 0 : VESA		

LVDS (Default VESA)

Note(19)

Auto Blanking : 0x0F											
1 Byte Data Length											
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0		D7~D4	Unused
										D3~D0	
										0 : Default 1 : Default+3frame delay 2 : Default+6frame delay 3 : Default+9frame delay 4 : Default+12frame delay 5 : Default+15frame delay 6 : Default+18frame delay 7 : Default+21frame delay 8 : Default+24frame delay 9 : Default+27frame delay A : Default+30frame delay	

Auto Blanking (Default off)

III. Input Format Setting

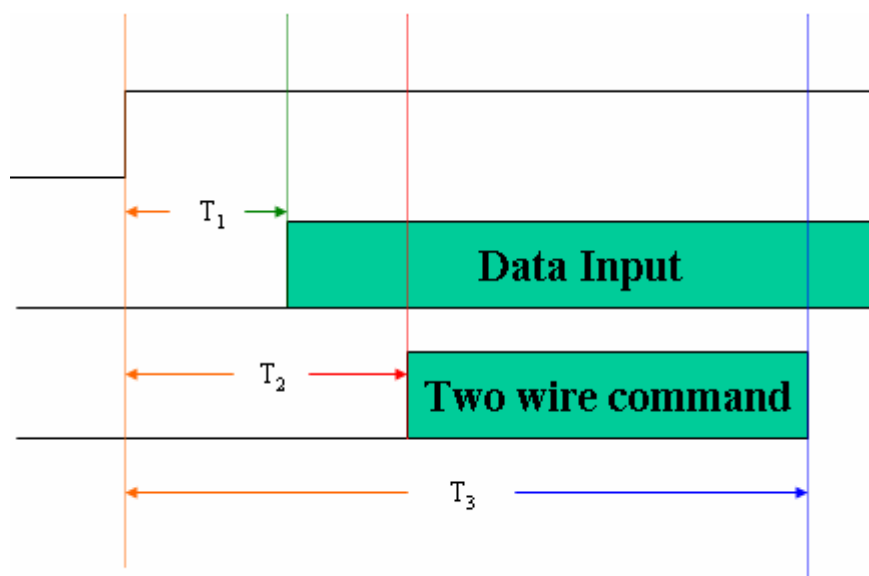
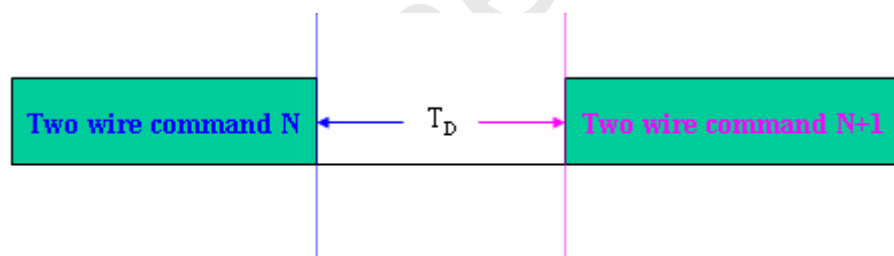
Command		Access Mode	Description	Remark
Input format setting	0x10	W	Input format setting select	Note(20)

Note(20)

Input Format Setting : 0x0F											
1 Byte Data Length											
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0		D7~D4	Unused
										D3~D0	
										0 : MEMC off (2D)@PAL system(50Hz) 1 : MEMC on (2D)@PAL system(50Hz) 2 : MEMC off (2D)@NTSC system(60Hz) 3 : MEMC on (2D)@NTSC system(60Hz) 4 : 2D convert 3D on &MEMC off (3D)@PAL system(50Hz) 5 : 2D convert 3D on &MEMC off (3D)@NTSC system(60Hz) 6 : SBS on &MEMC off (3D)@PAL system(50Hz) 7 : SBS on &MEMC off (3D)@NTSC system(60Hz) 8 : 720P FS on &MEMC off (3D)@100Hz 9 : 720P FS on &MEMC off (3D)@120Hz A : 1080P FS on &MEMC off (3D)@48Hz B : 1080P FS on &MEMC on (3D)@48Hz	

A.6 TWO WIRE BUS REQUIREMENT

Symbol	Parameter	Condition	Min	Max	Units
V_L	Input Low-voltage		0	0.7	V
V_H	Input High-voltage		2.7	3.3	V
$V_{hys}^{(1)}$	Hysteresis of Schmitt Trigger Inputs		0.16	—	V
$V_{OL}^{(1)}$	Output Low-voltage	9 mA sink current	0	0.4	V
$t_r^{(1)}$	Rise Time for both SDA and SCL		$20 + 0.1C_b^{(3)(2)}$	900	ns
$t_{of}^{(1)}$	Output Fall Time from V_{IHmin} to V_{ILmax}	$10\text{ pF} < C_b < 400\text{ pF}^{(1)}$	$20 + 0.1C_b^{(3)(2)}$	250	ns
$t_{sp}^{(1)}$	Spikes Suppressed by Input Filter		0	50 ⁽²⁾	ns
I_i	Input Current each I/O Pin	$0.1V_{CC} < V_i < 0.9V_{CC}$	-10	10	μA
$C_i^{(1)}$	Capacitance for each I/O Pin		—	10	pF
f_{SCL}	SCL Clock Frequency	$f_{CK}^{(4)} > \max(16f_{SCL}, 250\text{kHz})^{(5)}$	0	400	KHz
R_p	Value of Pull-up resistor	$f_{SCL} \leq 100\text{ KHz}$	3000	$\frac{1000\text{ns}}{C_b}$	Ω
		$f_{SCL} > 100\text{ KHz}$	3000	$\frac{900\text{ns}}{C_b}$	Ω
$t_{HD,STA}$	Hold Time (repeated) START Condition	$f_{SCL} \leq 100\text{ KHz}$	4.0	—	μs
		$f_{SCL} > 100\text{ KHz}$	0.6	—	μs
t_{LOW}	Low Period of the SCL Clock	$f_{SCL} \leq 100\text{ KHz}^{(6)}$	4.7	—	μs
		$f_{SCL} > 100\text{ KHz}^{(7)}$	1.3	—	μs
t_{HIGH}	High period of the SCL clock	$f_{SCL} \leq 100\text{ KHz}$	4.0	—	μs
		$f_{SCL} > 100\text{ KHz}$	0.6	—	μs
$t_{SU,STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100\text{ KHz}$	4.7	—	μs
		$f_{SCL} > 100\text{ KHz}$	0.6	—	μs
$t_{HD,DAT}$	Data hold time	$f_{SCL} \leq 100\text{ KHz}$	0	3.45	μs
		$f_{SCL} > 100\text{ KHz}$	0	0.0	μs
$t_{SU,DAT}$	Data setup time	$f_{SCL} \leq 100\text{ KHz}$	250	—	ns
		$f_{SCL} > 100\text{ KHz}$	100	—	ns
$t_{SU,STO}$	Setup time for STOP condition	$f_{SCL} \leq 100\text{ KHz}$	4.0	—	μs
		$f_{SCL} > 100\text{ KHz}$	0.6	—	μs
t_{BFC}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100\text{ KHz}$	4.7	—	μs
		$f_{SCL} > 100\text{ KHz}$	1.3	—	μs

A.7 THE TWO WIRE BUS SEQUENCE**I. Initial state** T_1 T_2 T_3 : TBD**II. Stable state** T_D : TBD